TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE MANUAL

TEST SET, INTEGRATED CIRCUIT CARD AN/USM-371 (Dynatronics Model ICT-102) (NSN 6625-00-431-8440)

H E A D Q U A R T E R S , D E P A R T M E N T O F T H E A R M Y

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OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE MANUAL FOR TEST SET, INTEGRATED CIRCUIT CARD AN/USM-371 (Dynatronics Model ICT-102) (NSN 6625-00-431-8440)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications and Electronics Materiel Readiness Command and Fort Monmouth, ATTN: DRSEL-ME-MQ, Fort Monmouth, New Jersey 07703.

In either case, a reply will be furnished direct to you.

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GENERAL

0-1 PRINTED CIRCUIT CARDS TESTED WITH THE AN/USM-371 and AN/USM-371A and ASSOCIATED TECHNICAL BULLETINS.

a. The following printed circuit cards are tested with the Test Set, Integrated Circuit Card AN/USM-371 and AN/USM-371A. Also listed are the associated technical bulletins containing the test set supplementary operating instructions and test programs used for these printed circuit cards.

Printed Circuit Cards	Technical Bulletin
A52602 through A65089	TM 11-6600-252-10-1 (Volume I)
A65093 through A65441	TB 11-6600-252-10-2 (Volume II)
SM-E-546367 through SM-E-546584	TB 11-6600-252-10-3 (Volume III)
SM-E-546587 through SM-E-546840	TB 11-6600-252-10-4 (Volume IV)
11153G1 through 56736G1	TB 11-6600-252-10-5 (Volume V)
PL-1139/G through PL-1158/G, and A-1 (MD-674) through A-33A2 (MD-674)	TB 11-6600-252-10-6 (Volume VI)
200000G1 through 200160G1, and PL-1119/G through PL-1124/G (SN-394)	TB 11-6600-252-10-7 (Volume VII)

b. The repair parts and special tools list technical manual for the AN/USM-371 is TM 11-6625-2577-24P.

NOTE

The technical manual for the Test Set, Integrated Circuit Card AN/USv-371A (Dynatronics Model ICT-103) is TM 11-6625-2594-14.

0-2 INDEXES OF PUBLICATIONS.

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

b. DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

0-3 MAINTENANCE FORMS, RECORDS, AND REPORTS.

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System.

b. Report of Packaging and Handling Deficiencies. Fill out and forward DD Form 6 (Packaging Improvement Report) as prescribed in AR 700-58/NAVSUPINST 4030.29/AFR 71-13/MCO P4030.29A, and DLAR 4145.8.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19C, and DLAR 4500.15.

0-4 REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR).

If your Test Set, Integrated Circuit Card AN/USM-371 needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Tell us why a procedure is hard to perform. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications and Electronics Materiel Readiness Command and Fort Monmouth, ATTN: DRSEL-ME-MQ, Fort Monmouth, New Jersey 07703. We'll send you a reply.

0-5 DESTRUCTION OF ARMY ELECTRONICS MATERIEL.

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

SECTION I
GENERAL DESCRIPTION

1-1 INTRODUCTION,

Dynatronics model ICT-102 Printed Circuit Card Tester (figure 1-1) provides the capability for dynamically testing virtually any logic card family on a visual GO/NO-GO basis. Punched (Hollerith) card programming for testing of TTL, DTL, RTL and discrete digital logic eliminates elaborate test hook-ups and engineering test analysis by high level engineering personnel. Simple to operate and program, this general purpose card tester is specifically designed for operation by unskilled personnel and programming by maintenance level technicians. No external test equipment is necessary because complete dynamic tests are performed by the Card Tester each time an individual program card is inserted into the card reader. All conditions (signal generation, power distribution, grounding, loading, test rates, etc.) are controlled by the program card and all circuits are fully tested by following a simple set of instructions and observing the GO/NO-GO and INPUT FAULT indicator lamps on the front panel. All front panel operator controls are for analytical purposes only thus, eliminating the possibility of operator error (and possible damage to circuits under test) attributed to improper switch settings. Worst case conditions are easily simulated through the use of programmable power supplies for marginal testing under dynamic conditions. Obsolescence of the card testing capability is eliminated by the inherent flexibility of the Card Tester which may be programmed to accommodate new circuit designs.

Functional checks on analog printed circuit cards are possible with

Figure 1-1. Card8ester, Model ICT-102

the Card Tester if used in conjunction with laboratory test equipment. In this case the Card Tester is used for test signal generation, test signal routing and power distribution. Because the unit is punched card programmable it is particularly useful for equipment repair, assembly line testing, quality control programs, on-site inspections, laboratory signal generator for breadboard designs, and general purpose signal generating requirements. Printed circuit card adapters are available for mating the card under test with the Card Tester CARD IN TEST connector. These PC card adapters are available as an option and determined by individual customer requirements.

1-1.1 SCOPE OF MANUAL. This manual was prepared by Dynatronics, an operation of the Electro Dynamic division of GENERAL DYNAMICS, and contains information required for operation, installation, and field maintenance of the model ICT-102 Printed Circuit Card Tester. Complete descriptions and examples of existing programs are also provided to illustrate the necessary programming procedures required to prepare printed circuit card test programs for the user's printed circuit cards. The contents of this manual include detailed operation and maintenance procedures for all subunits within the model ICT-102 providing a complete and concise document. Information pertaining to specific printed circuit card family programming and card testing procedures is normally located in a separate manual as determined by the individual contract. Each printed circuit card in the model ICT-102 has a program prepared which fully exercises the card under dynamic test conditions. These programs are fully documented in section IX of this manual.

1-1.2 PURPOSE AND USE OF CARD TESTER. The Card Tester is a compact, portable test instrument designed for use as a maintenance support equipment for off-line testing and repair of circuit modules. In this application the Card Tester is used to quickly locate the defective printed circuit card, which may then be replaced in the prime system. Trouble analysis and repair of the defective

printed circuit card may then be performed on the Card Tester after the prime system has been restored to operation. Because of extremely flexible programming parameters, the Card Tester is inherently suitable for GO/NO-GO testing TTL DTL, RTL and discrete digital logic modules and printed circuit cards.

1-2 PHYSICAL DESCRIPTION.

The Card Tester is available as a rack mount model ready for installation into "system" type configurations or as a bench model with optional portable cabinet. Each rack mount unit has provisions for mounting chassis slides to facilitate installation and maintenance. Optional accessories include a built-in Hollerith card storage drawer, plug-in output loads, extender card, extender cable, and card adapters. Detailed descriptions of the above mentioned options are delineated in the following paragraph.

1-2.1 MECHANICAL DESCRIPTION. The Card Tester is packaged in a single unit and can be easily configured for bench top laboratory use by adding the optional portable cabinet. The rack mount model is designed to fit into a standard 19-inch equipment rack and requires 7.0 inches of front panel space. Each portable cabinet is provided with a tilt stand to allow adjusting the Card Tester for optimum operator comfort while testing printed circuit cards. All circuitry, with the exception of front panel mounted controls and indicators, is contained on removable printed circuit cards. Access to the printed circuit cards and card test points is from the top of the chassis, and the chassis wiring is accessible from the bottom of the unit.

All controls used directly by the operator are located on the front panel of the unit. These controls are for analytical purposes only and eliminate the possibility of operator induced damage due to improper switch settings. Front panel controls consist of a card reader actuating handle, card test connector, IN/OUT selector switches, GO/NO-GO test indicators, INPUT FAULT indicator WAVEFORM TEST switches, external input connectors, IN/OUT monitor test

points, and internal test signal test points. Detailed descriptions of these controls and indicators are provided in section III of this manual.

Options to the basic Card Tester configuration consist of the following:

a. Portable Cabinet-A portable cabinet is available to fully enclose the Card Tester when used as a bench top testing device for laboratory use. Each cabinet is provided with an adjustable tilt stand to allow the operator to control the height of the unit thus, ensuring maximum operator comfort during testing operations. Two recessed flush mount handles are 'attached to each cabinet which allow convenient relocation of the Card Tester within a particular test facility.

b. Hollerith Card Storage Drawer-Optional storage drawer provides instant location of test program cards for up to 175 test programs. This storage drawer is located directly below the CARD IN TEST connector on the front panel of the unit.

c. Programmable Loads-Programmable load cards are provided to allow selection of card under test output circuit loads to properly exercise the tested circuits under compatible load conditions. The programmable load resistors are located on removable printed circuit boards which may be substituted, should the need arise, for selecting load resistors of different values to accommodate testing cards belonging to distinct card families with the same Card Tester. Additional programmable load cards are available as an option and the customer must determine the load resistor values for the two programmable load resistor printed circuit boards supplied with the Card Tester. Standard load resistor values are readily available for commonly used integrated circuit card families such as TI 5400 and 7400 series and their equivalent.

d. Card Adapters-Card adapters are available to interface a specific type of card-under-test to the front panel connector or to the receptacle on the flexible extender cable. This adapter makes it possible to interface the Card

Tester signals, power and loads with virtually any card family in existence.

e. Extender Cable-Flexible extender cables are available to allow the operator/technician perform troubleshooting steps on both sides of the printed circuit card under test. The plug end of the extender cable mates with the CARD IN TEST connector on the front panel, and the receptacle end of the cable is identical in pin configuration to the CARD IN TEST connector located on the front panel. Various lengths of extender cables are available to accommodate most situations.

1-2.2 DIMENSIONS AND WEIGHT. The outside dimensions of the Card Tester are slightly different for each model and are listed below:

Bench Top Model (with portable cabinet):
a. Height-8-1/2 inches
b. Width-19-3/4 inches
c. Depth-18 inches

Rack Mount Model:
a. Height-7 inches
b. Width-19 inches
c. Depth-18-5/8 inches

The approximate weight of each unit is listed below.
a. Rack Mount Unit-45 pounds
b. Bench Top Unit-65 pounds

1-3 FUNCTIONAL DESCRIPTION.

The Card Tester functions as a programmable signal generator used to dynamically exercise the digital circuits contained on printed circuit cards. An internal clock and test signal generator (figure 1-2) are controlled by the program card and provide the source of signals to be applied as stimuli to the card under test. Signals to be used as inputs to the circuits being tested are selected via the punched card in the card reader matrix and routed through the programmable drivers. These programmable drivers are also set up by the program at the proper

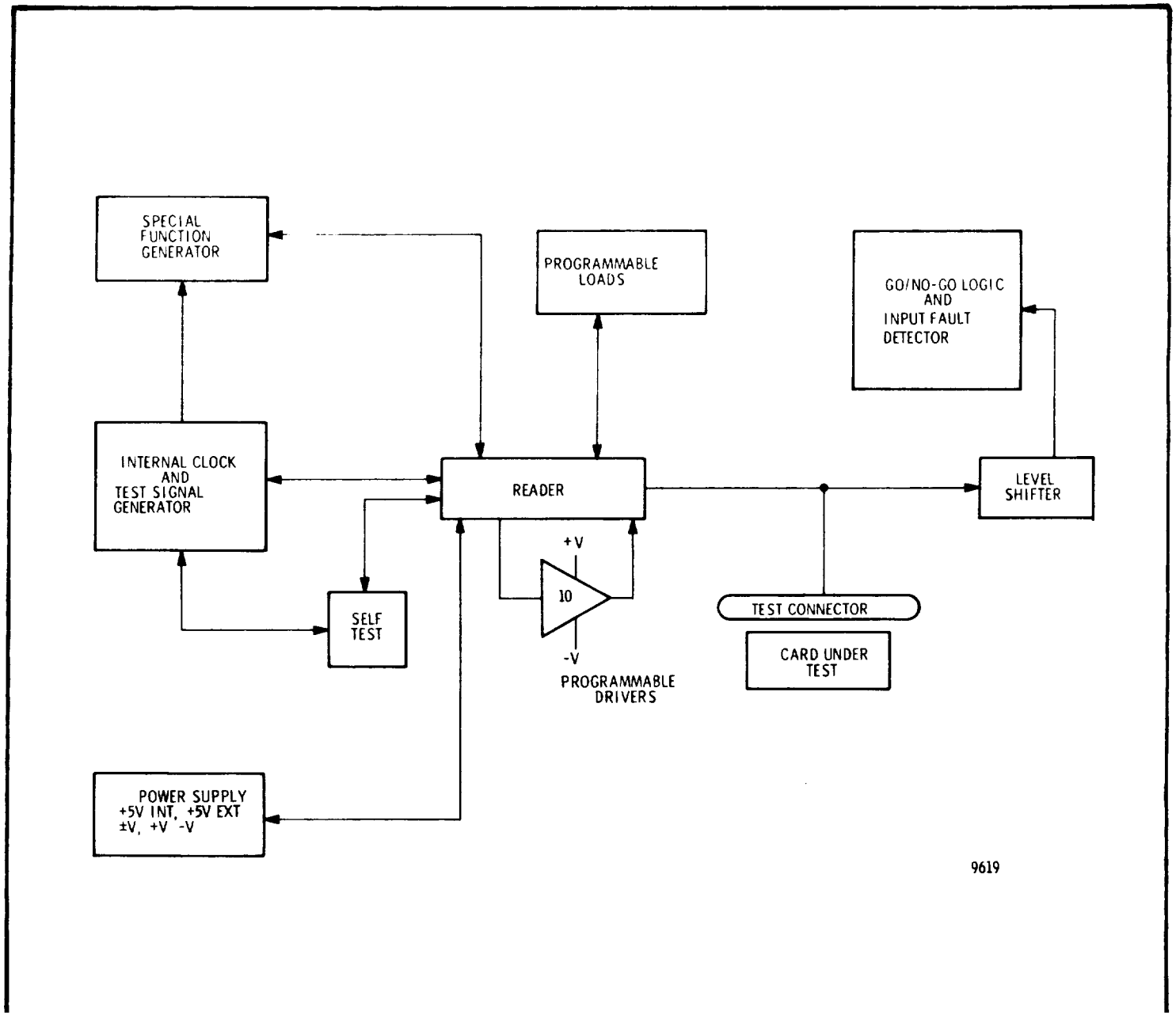


Figure 1-2. Card Tester, Simplified Block Diagram

signal levels required to exercise the circuits under test. Any signal thus selected is routed out of the card reader matrix to any combination of input pins on the card being tested. By this method, any ten of the available test signals, power or ground may be applied to any combination of pins on the card being tested to fully exercise sequential and combinational logic or signal handling circuits. Likewise, under program control, any outputs of the card under test are loaded to simulate actual circuit characteristics.

The GO/NO-GO circuits operate on the principle of interval measurements between distinct edges (transitions) of the output signals of the card being tested. For each output signal of a card, the operator selects, as called for in the test instructions, a portion of the output signal and the required interval. Proper operation for that portion of the signal is evidenced by a GO lamp, and incorrect operation results in lighting a NO-GO lamp.

The GO/NO-GO testing display is augmented by an input fault lamp which automatically provides an indication of a faulty test signal into the card under test caused by shorting of a test signal to another test signal or to a power or ground bus.. A detected input fault inhibits only the affected programmable driver(s) while maintaining all other test signals and voltages into the card under test. This method reduces troubleshooting time by isolating the malfunctioning input of the circuit under test.

Self test capability is simple and conclusive, since it uses the same circuits and signal checking techniques for operational testing. The following paragraphs provide detailed descriptions of the major subunits within the Card Tester.

1-3.1 CARD READER. The card reader provides a 12 X 80 matrix used to distribute control parameters, internally generated test signals, power and ground to circuits within the Card Tester and to 'the printed circuit card under test. Individual programs are punched onto standard Hollerith 12 X 80 tabulating cards which are inserted into the card reader making the necessary internal connections in the reader. Insertions of a test program card into the reader

automatically energizes the Card Tester and provides the following functions for the Card Tester and printed circuit card under test:

a. Clock Cycle Frequency
b. Bit Counter Interval
c. Test Signal Generation
d. Test Signal Distribution
e. Power and Ground Distribution
f. Programmable Power Supply Voltages
g. Test Signal Logic Levels
h. Card-Under-Test Output Loads
i. Card-Under-Test Level Shifter Threshold

1-3.2 CLOCK SIGNAL GENERATION. The basic timing for generation of interval test signals is supplied by a 4 MHz oscillator which is counted down digitally to derive four separate test clock cycle periods of 1 usec, 2 usec, 32 usec and 16 Msec. Selection of a particular clock rate is controlled by the programming on the Hollerith card. Once one of the four test clock cycle periods has been selected all internally generated test signals are derived from the basic clock rate. The selected test clock rate is gated into the first stage of the eight-stage "B" test signal generation counter.

1-3.3 TEST SIGNAL GENERATION. Test signals consist of three distinct groups of phase related signals (18 signals total) in addition to the provisions for routing various power, ground, and external inputs into the card under test. These three groups include "B" test signals, "C" test signals and special function test signals (+SO through +S2). "B" type test signals are derived from one of the four selected basic clock rates by digitally stepping the basic clock rate down through an eight-stage binary counter. Each stage of the eight-stage counter provides a unique output which is identified as +BO through +B7. Outputs from the "B" test signal generator are applied to the "C" test signal generator, producing seven unique test signals which are phase shifted in order that the "B" and "C" test signal transitions are non-coincident. These test signals provide selected control pulses used for gating and strobing which are not edge coincident

with the "B" test signals thus permitting gating and clocking operations without generating spurious pulses (slivers). The third group of test signals are referred to as special function test signals (SO, S1, S2) and are generated by programming any one or combination of three basic logic circuits to produce a desired special test signal. The special function generator consists of a flip-flop/AND/NOR combination with all inputs independently programmable for generation of unique test signals.

The total of 18 test signals (eight "B", seven "C", and three "S") are available of which any combination of 10 can be switched through the card reader to the programmable drivers and thence to the printed circuit card under test. Four of these test signals (any four as determined by the programmer) may be inverted, under control of the program card.

1-3.4 PROGRAMMABLE DRIVERS. Ten programmable drivers are located in the card tester to provide a program controlled signal buffer to output unipolar signal levels up to 24 volts peak (either negative or positive) or 30 volts peak to peak symmetrical or nonsymmetrical bipolar outputs. The programmable drivers are used to level shift the internally generated test signals for compatibility with the input requirements of the card under test. Each driver output circuit is a complementary pair, each end of which is referenced by the program card to power supply busses or ground, thereby setting the logic levels at the driver outputs. Any one of the 18 test signals generated by the test signal generator can be applied to any of the ten programmable drivers via the program card. Four of the programmable drivers contain a signal inverter prior to the input which, under control of the program card, cause the selected test signal to be inverted before being applied to the driver input. This inverted test signal is then buffered by the driver and applied to the appropriate input(s) of the card being tested. When not selected under program control, the inverter circuits pass the selected test signal directly (no inversion) into the programmable driver input.

1-3.5 PROGRAMMABLE LOADS. Programmable load resistors (resistor value determined by customer requirements) are supplied with each Card Tester which

are used to load the circuit(s) under test (under program control via the card reader). The load resistors are physically located on two removable printed circuit cards to allow for convenient changeover between various card families being tested by the same Card Tester. Each resistor on either card may be programmed to any programmable pin on the card under test (via the CARD IN TEST connector). On one of the load resistor cards, all resistors are returned to +5V while on the second load resistor card the resistors are returned to any of the power supply outputs or ground, under control of the program (IBM Card).

1-3.6 GO/NO-GO LOGIC. The GO/NO-GO logic automatically compares the precise time interval between distinct edges (transitions) of the output signal to the circuit under test. This measurement provides a concise indication as to whether or not the circuit under examination is functioning according to its design requirements. Each output from the printed circuit card under test is selected by the operator and dynamically exercised and accurately measured by the GO/NO-GO logic circuits to ensure the validity of the output signal.

Basically the GO/NO-GO circuits consist of an edge counter and comparator, bit counter and comparator, GO flip-flop, NO-GO flip-flop and end-of-frame no-go detector. These circuits are used in conjunction with the A (edge) and B (bit count) selector switches to determine the validity of each output signal transition. In addition, the Card Tester automatically checks for input faults (caused by inputs shorted to other test signals or either power or ground busses) and if an input fault is detected, automatically disables the affected test signal programmable driver and lights the front panel INPUT FAULT indicator. Once an input fault is detected the GO flip-flop is locked out until either the input fault is corrected or the Card Tester is reset. By determining which input signal to the card under test is faulty, the operator can quickly isolate the shorted input circuit and determine the cause of the input fault malfunction.

1-3.7 SELF TEST. Self Test in the Card Tester is accomplished in two phases.

The first phase utilizes the internal GO/NO-GO logic to verify the correct timing of each internally generated test signal in the same manner as used to determine the validity of an output signal under test. A programmed Hollerith card is provided which allows the operator to select, on the pin selector switches each test signal and to perform the test sequence on the waveform test switches while observing the GO/NO-GO indicators.

A second self test capability provides a rapid means of self-verifying that the majority of internal functional circuits operate as designed. This phase of the self test procedure also provides a fault isolation capability when used in conjunction with the troubleshooting procedures location in section V of this manual. A programmed Hollerith card is supplied which when inserted into the card reader prepares the Card Tester for the self test procedure. The operator then sequentially selects TEST positions 1 through 4 on the TENS switch while interpreting the condition of the GO/NO-GO indicators in each position. Each step in the sequence builds confidence in each major functional area of the Card Tester. Instructions for self test operation and Card Tester malfunction analysis are provided in detail in section III and section V respectively.

1-3.8 POWER SUPPLY. All Card Tester internal voltages and voltages required to operate cards under test are supplied by a completely self contained internal power supply module which operates from a 115 VAC power source. This self contained power supply consists of two +5 volt power supplies, one -6 volt power supply, one +12 volt power supply and three programmable power supplies which are described in detail below.

1-3.8.1 Internal Power Supplies. All voltages required for operation of internal Card Tester circuits are listed below:

a. +12 VDC power supply This power supply provides +12 volts DC to the four indicators located on the front panel and to the internal line receivers for bias purposes. Plus 12 volts is not available to be programmed into the printed circuit card under test. One output line from the +12 volt power supply is protected with a 3/4 amp fuse and supplies power to the indicators mentioned

above.

b. -6 VDC power supply - Minus 6 volts 1)(is used for the internal Card Tester line receivers and is not available for Use in the card under test.

c. +5 VDC Internal (INT) power supply All integrated circuits used within the Card Tester operate from the internal +5 volt DC power supply. This supply is independent from the +5 volt external power supply to prevent losing Card Tester power in the event of an external power supply short caused by the printed circuit card under test. The internal +5 volt power supply has an adjustable range from +4.5 volts to +5.5 volts and supplies up to 1 ampere. Overvoltage protection consists of a crowbar circuit which clamps the output voltage to zero volts if the output voltage increases to +7.0 volts.

1-3.8.2 +V Programmable Power Supply. The plus voltage (+V) power supply and regulator are programmable in 100 mv steps from .5 volt to a maximum of +26X1 volts DC. Up to 800 ma output current is available from the +V power supply which supplies voltage to the card under test, internal level shifter (if programmed), internal line receivers (if programmed) , card location 8A (if required for load resistor reference voltage), and to the programmable drivers (as determined by the required test signal levels input into the card under test).

1-3.8.3 -V Programmable Power Supply. The minus voltage (-V) power supply and regulator are identical to the +V power supply described above except the output voltage is a negative voltage. Minus V power supply usage is also the same as for the +V power supply described above.

1-3.8.4 +V Programmable Power Supply. This power supply is identical to the + and -V power supplies described above with the added feature of output voltage polarity control via the program card. Also, the $\pm$V supply is capable of either sourcing or sinking current and therefore is normally used at the clamp voltage for testing discrete component logic circuits. The output voltage (1 volt through 26.1 volts) polarity is determined by the operators program card and can be either positive or negative. Power distribution for this supply is identical to both the + and -V power supply output voltages.

1-3.8.5 +5V External (EXT) Power Supply. The +5V external power supply is identical to the +5V INT power supply (paragraph 1-3.8.1 (e)) except for the output voltage distribution. Distribution for the +5V EXT output voltage includes the CARD IN TEST connector on the front panel, Row 10 of the card reader (for connection to the card under test if required on input pins other than pin 54, and to printed circuit card location 9A where +5V EXT is connected to the common side of the load resistors. An adjustment is provided through a slot in the rear of the chassis for controlling the output voltage range from +4.5 volts DC to +5. 5 volts DC. Overvoltage protection consists of a crowbar circuit which clamps the output voltage level to zero if the output voltage increases to +7.0 volts. Output current limits after approximately 1 ampere.

1-4 CONDENSED DATA.

1-4.1 SPECIFICATIONS AND FEATURES. Table 1-1 below summarizes the Card Tester specifications, features and options.

Table 1-1. Specifications and Features

PARAMETER	SPECIFICATIONS
TEST SIGNALS	
CLOCK SOURCE	Four test rates - 1 usec, 2 usec, 32 usec, and 16 Msec selected by program card.
SIGNAL GENERATOR	18 Test Signals Total
"B" Test Signals	Eight test signals generated by an eight stage binary counter which divides the selected basic clock rate.
"C" Test Signals	Seven test signals derived from "B" test signals to provide strobes, resets, gate pulses etc. All "C" test signals are non-coincident with respect to the "B" test signals.

Table 1-1. Specifications and Features (Cont'd)

PARAMETER	SPECIFICATIONS
SIGNAL GENERATOR (Cont'd)	
Special Function Test Signals	Three basic logic elements (flip-flop, AND gate and NOR gate) with inputs under operator control via punched program card. Input test signals to special function elements are "B" and "C" test signals.
TEST SIGNAL LEVELS	Programmable in 100 millivolt steps to +24 volts unipolar or 30 volts peak-to-peak symmetrical or nonsymmetrical.
TEST CONNECTOR	56-Pin, 54 of which are independently programmable to any of the 18 test signals, programmable voltages, output circuit loads, or system ground. Two pins are dedicated to logic power (pin 54) and ground (pin 56).
Adapters	Adapters are available to accommodate various printed circuit card family connectors. These adapters are available as an option to the Card Tester and fabricated according to customer requirements.
PROGRAMMING	
FORMAT	Simple to program using non-computer programming terminology and methods. Easy to program - instructions and actual program examples are included in this manual. Adapts well to customer requirements thus eliminating equipment obsolescence due to new printed circuit card design and improved circuits.

Table 1-1. Specifications and Features (Cont'd)

PARAMETER	SPECIFICATIONS
PARAMETERS	
I/O	Any single pin, or combination of pins, can be programmed with: Test Signals Programmable Voltages System Ground Externally Generated Signals Inverted Test Signals Programmable Loads
Test Rate	Four test rates are programmable as listed: 1 usec 2 usec 32 usec 16 usec
Special Function Signals	Three basic logic elements (flip-flop, AND gate and NOR gate) with inputs under operator control via punched program card.
Test Signal Levels	See TEST SIGNALS, TEST SIGNAL LEVELS
Power Supply Voltages	Three internal power supplies are under program control to provide the following programmable voltages: -V Power Supply - Programmable in 100 millivolt steps from -0.5V to -26.1 +V Power Supply - Programmable in 100 millivolt steps from +(Q.5V to +26olV ±V Power Supply - Programmable in 100 millivolt steps from 1.0V to 26.1V, Output voltage polarity is also under program ,control. A fourth power supply (+5V EXT) can be input to any of the 54 pins on the CARD IN TEST connector.

Table 1-1. Specifications and Features (Cont'd)

PARAMETER	SPECIFICATIONS
SELF TEST	
DIAGNOSTIC	Switch selectable internal self-test verifies functional operation of major logic circuits which comprise the Card Tester. Complete cause and cure tables are provided in section V to isolate problems detected during self-test operations.
CLOCK TIMING TESTS	A program card is provided to exercise all internally generated test signals allowing the operator to individually verify the timing of these test signals.
TEST AIDS	
Test Signal Test Point Points	All internally generated test signals are available for observation purposes at individual test points on the front panel.
GO/NO-GO indicators	Front Panel indicators provide positive indication of test results.
Power Supply output test points	Programmable power supply outputs, +5V internal, and +5V external power supply output voltages are available on individual test points located on the front panel.
Lamp test	Pressing the LAMP TEST indicator (POWER ON indicator) causes all indicators to illuminate.
Output Loads	Two resistors may be programmed to any of 54 pins to simulate nominal loads to the card-under-test.

Table 1-1. Specifications and Features (Cont'd)

PARAMETER	SPECIFICATIONS
TEST AIDS (Cont'd)	
Output Load Reference Voltage	One group of output loads (54 resistors) are commoned by a single line and, under program control, can be connected to the following: ±V, +V,-V Output Voltages +5V EXT output voltage System ground The second set of load resistors is returned to +5V EXT.
Level Shifter Threshold	Programmed to level shift card-in-test output signals from programmed level to TTL level signal before being applied to Card Tester GO/NO-GO logic.
CARD READER	12 row by 80 column matrix which accepts standard Hollerith tabulating cards or long lasting PVC program cards. Card reader matrix provides interconnection between internal signal control circuits, programmable power supplies and the card under test. The card reader automatically energizes the card tester each time a program card is inserted into the card reader slot and the actuating handle is rotated-to the right. Power will not be applied if the program card is mis-oriented,
HOLLERITH CARDS	Standard tabulating card with a "12" edge cut on the column 1 end. Program cards (standard tabulating cards) can either be punched using standard key punch equipment or by using the inexpensive portable hand punch listed in table 1-3.

Table 1-1. Specifications and Features (Cont'd)

PARAMETER	SPECIFICATIONS
POWER REQUIREMENTS	115 volts AC-:10%, single phase, at less-than 2.0 amperes. Line frequency range equals 45 through 450 Hz.
PHYSICAL CHARACTERISTICS	See paragraph 2-3.
WEIGHT	Portable Bench model - 65 pounds Rack mount model - 45 pounds
DIMENSIONS	
Portable Bench Model	Height - 8-1/2 inches Width - 19-3/4 inches Depth - 18 inches
Rack Mount Model	Height - 7 inches Width - 19 inches Depth - 18-5/8 inches

1-4.2 FUSE COMPLEMENT. There are two fuses located on the rear panel of the Card Tester which protect the power supply input transformer (AC input) and the +12 volt DC lamp power supply line. All other power supply circuits are short circuit protected and automatically recover after the cause of the shorted output has been corrected. Figure 7-13 illustrates the electrical circuits protected by F1 and F2.

Fuse functions and ratings are listed below:

a. F1 - AC input to internal power supply, PS1,2A, 3AG - Fast Blo.
b. F2 - + 12 volt DC lamp output protection, PS1, 3/4A, 3AG - Fast Blo.

1-4.3 PRINTED CIRCUIT CARD COMPLEMENT. All internal integrated circuit logic and discrete component circuitry is contained on printed circuit boards designed and manufactured by Dynatronics. These printed circuit boards are located in a single tray (tray A) and are numbered 1A through 9A. Table 1-2 provides the name, Dynatronics part number, physical location and quantity used per Card Tester for the total complement of printed circuit boards.

Table 1-2. Printed Circuit Card Complement

LOCATION	PART NUMBER	NAME	QTY
1A	08-890710-1 or -2	"B" Test Signal Generator	1
2A	08-890711-1 or -2	"C" Test Signal Generator	1
3A	08-890712-1 or -2	GO/NO-GO Test Logic	1
4A, 5A	08-890714-1 or -2	Programmable Drivers	2
CA	08-890716-1 or -2	Line Receivers	1
7A	08-890715-1 or -2	Input Fault Comparator	1
8A	08-890713-1 or -3	Load Resistor Board (3K ohm)	1
9A	08-890713-2 or -4	Load Resistor Board (510 ohm)	1

Identification of printed circuit boards throughout the manual refers to the last three digits of the part number and the dash number to the right of these digits. For example, the printed circuit board located in card slot 1A is referred to as the 710 card. Note that the dash number is omitted (assumed to be a dash 1) when the card referenced is a dash l' assembly. Card slot 9A contains a 713-2, for example. Complete printed circuit board descriptions and functional testing information is contained in section VIII of this manual. Section VIII provides the theory of operation, parts replacement tabulations, technical characteristics, schematic/logic diagrams, vender names and addresses

for ordering faulty components, and Card Tester information necessary for complete malfunction diagnosis pertaining to these cards.

1-4.4 POWER REQUIREMENTS. Table 1-1 lists the primary AC power requirements for the Card Tester.

1-5 TEST EQUIPMENT AND SPECIAL TOOLS

The following paragraphs describe the necessary special tools and test equipment required to maintain the Card Tester under normal operating conditions. Ordinary hand tools (usually found in laboratories supporting electronics equipments) are not listed below. Additional information is presented to describe the use of a portable IBM tabulating card punch which, is commercially available for use by customers not having access to a standard teletypewriter (normally used for punching program cards)

1-5.1 TEST EQUIPMENT. Test equipment, or equivalent types, required to mnaintain the Card Tester are listed below.

a. Oscilloscope, Tektronix, Inc., Type 545B with type 1A1 plug-in.
b. Volt/ohmmeter, Simpson, Model 269
c. Digital Voltmeter, Dymec 2401B.

1-5.2 SPECIAL TOOLS. Special tools required in addition to common laboratory hand tools are listed below.

a. Wire Wrap Gun with Battery, Gardner Denver, Type 14R2
   Sleeve - Gardner Denver, Part No. 502129
   Bit - Gardner Denver, Part No. 502128
b. Extender Board, Dynatronics, Part No. 08-900700

1-5.3 TABULATING CARD PUNCH. Economical program card punching operations are fully implemented with the use of a portable hand operated punch (figure 1-3). This particular model, Wright model 2600, accomplishes program card punching tasks with a minimum of operator effort thus, providing an efficient and practical punch for punching new, modified or experimental program cards. Even where a standard teletypewriter keyboard and IBM card punch are available, a portable manually operated unit will find ample use to justify the small investment required for the purchase of such a punch.

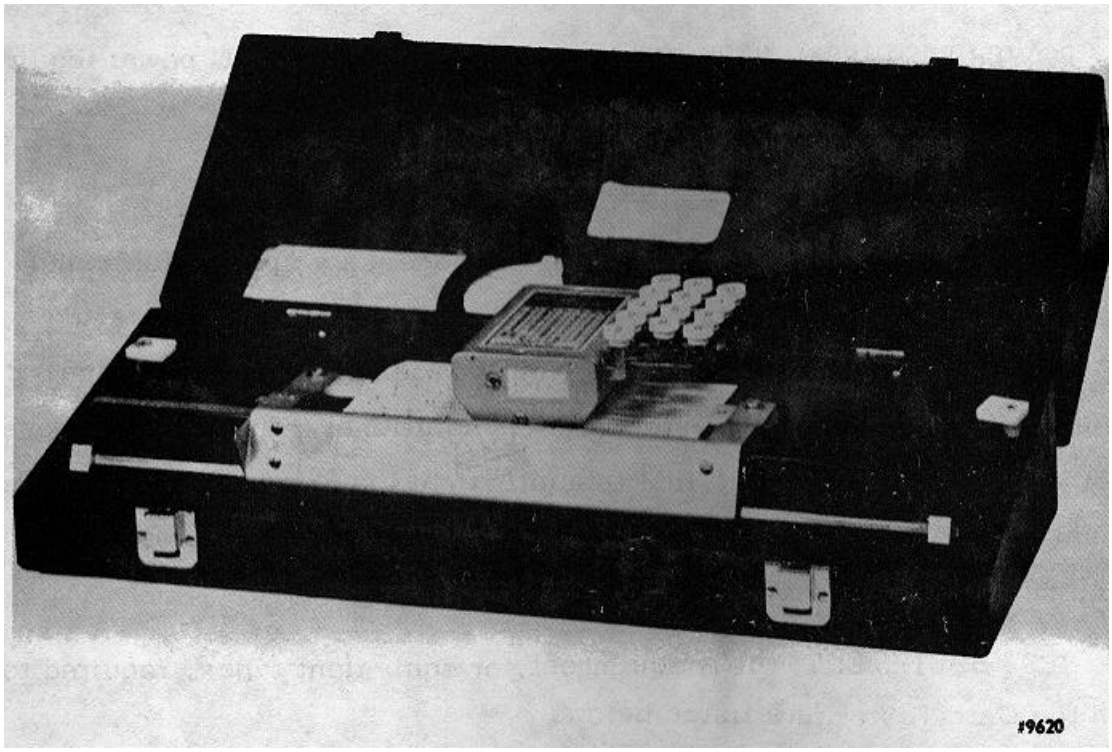


Figure 3. Typical Manually Operated IBM Card Punch.

OPTIONS.

Several Card Tester options are available to enhance its flexability and thus adapt itself will into most laboratory environments. The optional accessories and services described in the following paragraphs may be specified at the time of purchase or as required by the customer due to increased testing requirements.

PORTABLE CABINET. For applications requiring continued bench use, the Card Tester can be furnished with a portable cabinet which totally encloses the internal workings thus, protecting the unit from accidental damage caused by foreign objects falling into the unit. This attractive and functional cabinet features recessed carrying handles and adjustable tilt stand for convenient

portability and comfortable operator positioning. Custom color schemes are available upon request.

1-6.2 STORAGE DRAWER. Convenient finger tip location of program cards (Hollerith cards) is made possible through the use of the optional storage drawer located directly below the CARD IN TEST connector on the front panel of the Card Tester. Storage capacity of the drawer is approximately 175 program cards.

Note
If the storage drawer is desired, this option must be specified at the time of purchase.

1-6.3 PROGRAMMING SERVICE. Dynatronics will provide (upon request) an estimated cost for the programming necessary to fully test customer printed circuit cards. This cost estimate will be based on the printed circuit board descriptions and technical characteristics furnished by the customer. All programming solicited by Dynatronics will be performed by highly skilled engineering personnel proficient in the use of programming techniques employed by the Card Tester. Many circuits used in customer owned printed circuit boards are similar in function to circuits contained in Dynatronics printed circuit card family, already programmed to provide a store of programming techniques for these and other similar circuits. Also, Dynatronics offers coding forms and custom tailored training courses to facilitate rapid orientation of key personnel.

1-6.4 PROGRAMMABLE LOAD BOARDS. Printed circuit card families utilizing standard and non-standard components require unique characteristic load resistor values to properly exercise the circuits under maximum load conditions. Each Card Tester is furnished with two programmable load cards (resistor value determined by customer requirements). Additional programmable load cards, replacing existing load cards in a matter of seconds to accommodate unique printed circuit card families tested by one card tester, are available at a nominal cost to the customer. Each load resistor printed circuit board contains 54 resistors with one

side of each resistor commoned.

1-6.5 PRINTED CIRCUIT CARD ADAPTERS. Interconnecting various printed circuit card families with the Card Tester requires the use of a card adapter such as the one shown in figure 1-4. Individual printed circuit card adapters are furnished as an optional item and are priced according to their complexity. In most cases the card adapter is a simple variation of existing card adapters manufactured by Dynatronics and in some cases adapters are available which have already been designed and are being manufactured.

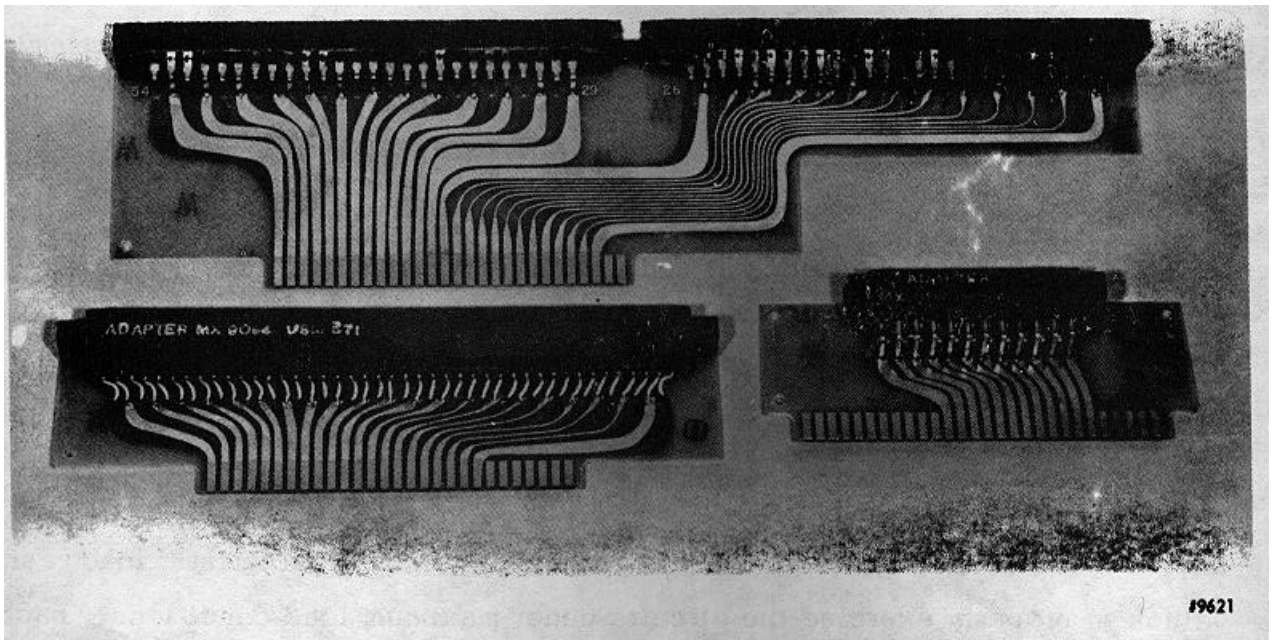


Figure 1-4. Typical Printed Circuit Card Adapters

SECTION II
INSTALLATION

2-1 INTRODUCTION.

This section contains the mechanical and electrical interface information required to install the Card Tester. No special instructions are necessary for installation of the bench top model. Specific instructions are provided for mechanical installation of the rack mount Card Tester, normally installed utilizing chassis slides for attaching the unit into the equipment rack. Numerous styles (for specific applications) of chassis slides are available and are readily adaptable to the Card Tester. Once installed, refer to section III for detailed operating procedures, self-test steps, and instructions for the preparation of punched cards (programming.)

2- 2 UNPACKING.

The Card Tester is shipped from the factory in a single container, fully assembled and is ready to be placed into operation after an initial inspection of the unit has been performed. After removal of the unit from the shipping container, inspect the chassis for damage that may have occurred in transit. Remove the portable cabinet (if supplied) and ensure that all printed circuit cards are properly seated.

2-3 MECHANICAL INSTALLATION.

2-3.1 BENCH TOP MODEL. There are no special procedures to follow when installing the bench top model Card Tester. Simply place the unit on the top of the bench, adjust the tilt stand if desired, and insert the AC power

cord into a bench or wall receptacle (wired for 115 VAC ±10% - see paragraph 2-4). Refer to section III for operating procedures and instructions for performing self test.

2-3.2 RACK MOUNT MODEL. Installation instructions for the rack mount Card Tester model are determined by the equipment rack structure and the type of chassis slides (or other method) used for installation. Installation details pertaining to the Card Tester chassis are shown in figure 2-1. Standard hole spacings, hole dimensions, etc., are used throughout. The Card Tester is designed for operation in a sheltered environment over the temperature range of 30°F to 130°F. The unit should be located such that ample free-air circulation is allowed around the chassis. External forced-air cooling is not required unless the Card Tester is placed in an enclosure with other heat producing equipment.

Note

When installing the Card Tester in an equipment rack with other electronic equipment, ensure that any equipment installed directly above the Card Tester does not protrude more than 1/4 inch beyond the front panel (in the area above the card reader handle). The card reader handle extends 1-3/4 inches above the front panel as it is turned to the open or closed positions. Refer to figure 2-2 for the dimensions and location of the card reader handle,

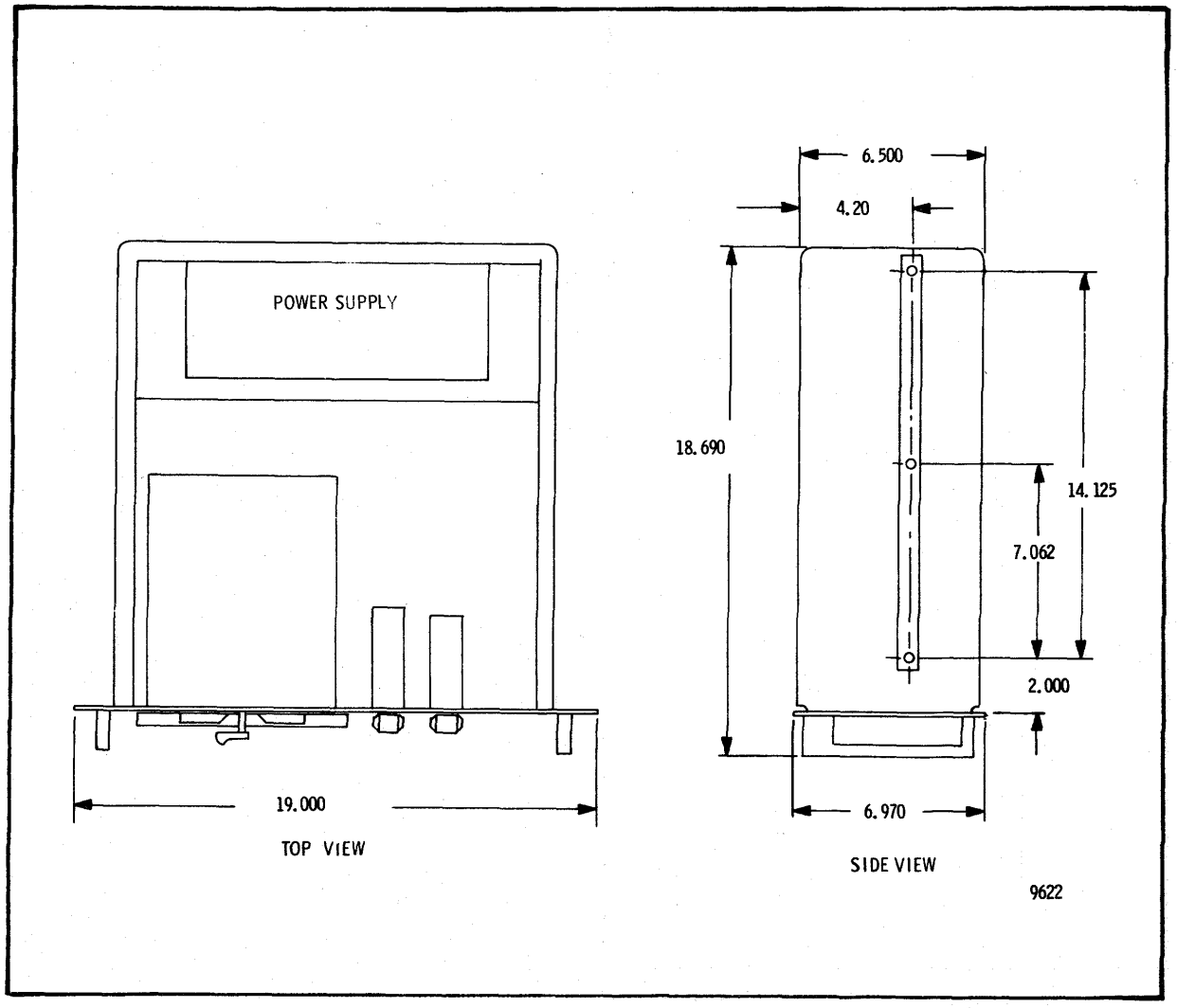


Figure 2-1. Rack Mount Model, Installation Details

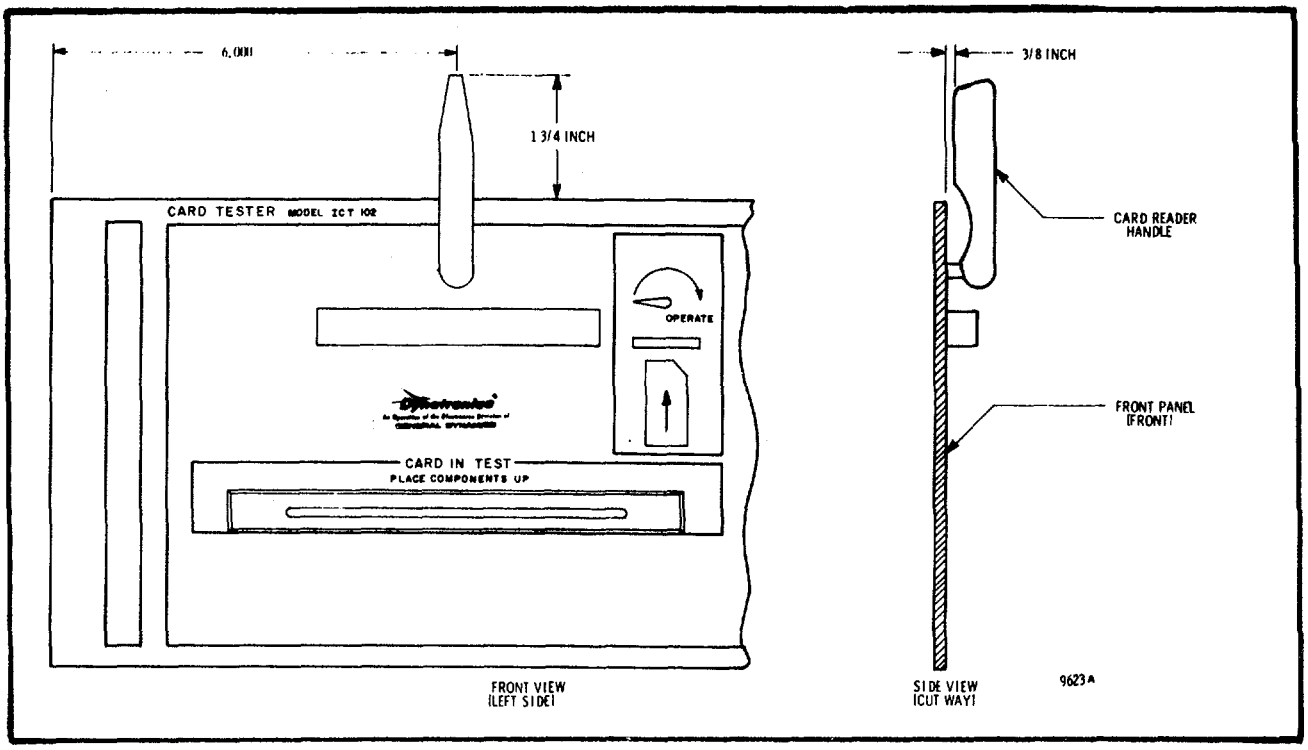


Figure 2-2. Card Reader Handle Location

2-4 ELECTRICAL INSTALLATION

Electrical installation consists of simply connecting the AC power cord to a single phase 115 VAC ±10% power source. The DC power supply module is protected (AC line) with a 2 ampere fast-blo fuse (F1). AC power is automatically applied to the Card Tester each time a programmed Hollerith tabulating card is inserted into the card reader.

2-5 INITIAL TESTS AND ADJUSTMENTS.

Perform the self-test procedure given in paragraph 3-4 to verify that the Card Tester is operating according to specifications. If a malfunction is determined during the self -test routine, refer to section V for further instructions and troubleshooting aids to determine the cause of the malfunction. The Card Tester is fully tested and adjusted at the factory and requires no further adjustments during installation unless repair work is performed in the power supply module.

the Card Tester is operating according to specifications. If a malfunction is determined during the self-test routine, refer to section V for further instructions and trouble shooting aids to determine the cause of the malfunction. The Card Tester is fully tested and adjusted at the factory and requires no further adjustments during installation unless repair work is performed in the power supply module.

SECTION III
OPERATION

3-1 INTRODUCTION.

This section describes the operator controls and indicators, operating procedures, self-test procedures, and instructions for preparation of card test programs (including examples of actual programs prepared for existing printed circuit cards). Instructions and examples given for programming are presented as a training aid to allow the operator, technician, or laboratory engineer to prepare Card Tester test programs for printed circuit cards with which he is familiar. Anyone with a basic knowledge of circuit operation can master the programming skill3 necessary for the operation of the Card Tester by following the steps presented in the following paragraphs.

3-2 CONTROLS AND INDICATORS.

All lamps,, switches, etc., requiring observation or manipulation by the operator are located on the front panel of the Card Tester. The front panel is illustrated in figure 3-1 and individual control and indicator descriptions are given in table 3-1. Before attempting to operate the Card Tester, carefully read the operating instructions delineated in paragraph 3-4. The operating instructions are provided as a guide to ensure successful testing results with a minimum of switch manipulation and indicator observance by the operator.

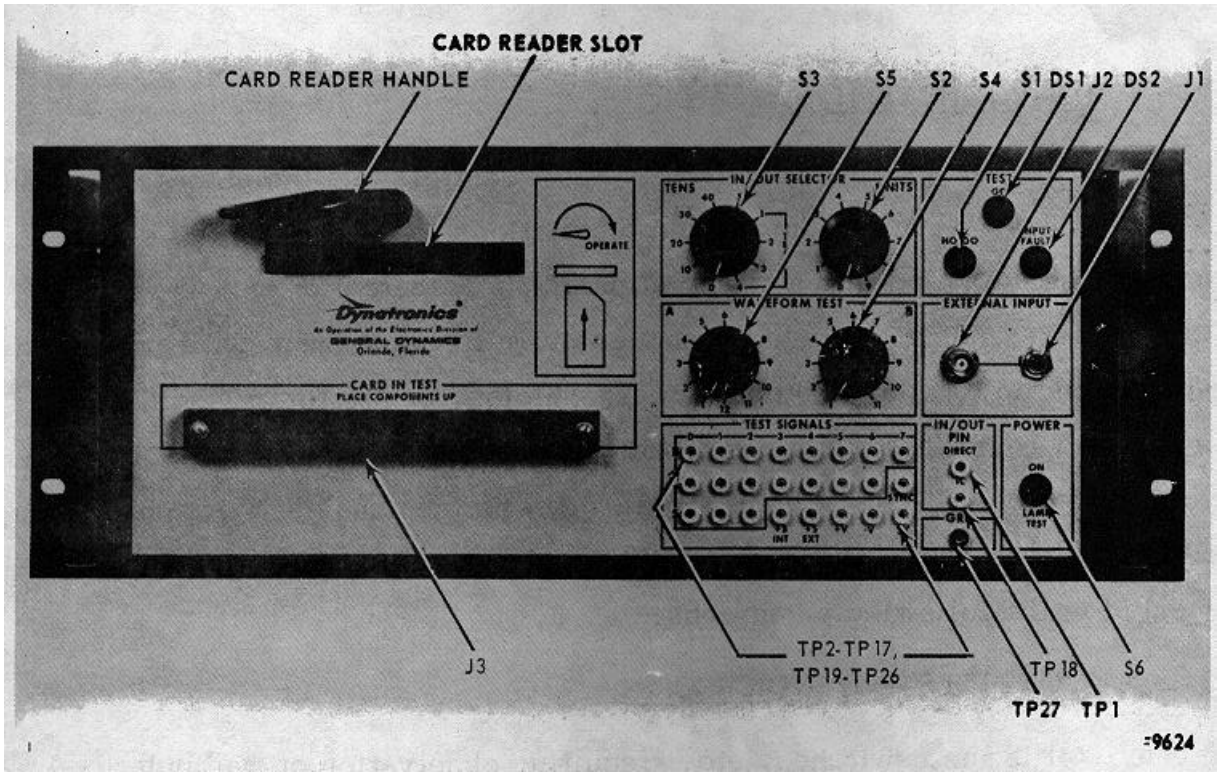


Figure 3-1. Card Tester Front Panel Layout

Table 3-1. Card Tester Controls and Indicators

NAME	REFERENCE DESIGNATION	FUNCTION
TEST GO indicator	DS1	Green indicator indicates a satisfactory time measurement for the edge being tested on the signal selected by the IN/OUT SELECTOR switches S2 and S3.
TEST INPUT FAULT indicator	DS2	Red indicator indicates shorted test signal inputs to the card under test or a shorted circuit on the printed circuit card being tested.
EXTERNAL INPUT audio connector	J1	Front panel audio connector (connected in parallel with BNC connector J2) for routing an external test signal to the card under test via the Card Tester.
EXTERNAL INPUT BNC connector	J2	Front panel BNC connector (connected in parallel with audio connector J1) for routing an external test signal to the card under test via the Card Tester,
CARD IN TEST connector	J3	56-pin test connector receives printed circuit card to be tested. Also interfaces printed circuit card adapters and extender cable. Fifty-four of the 56 pins are under control of the Card Tester (programmable) to supply test signals to the card under test. Pin 54 is wired to the +5V EXT power supply output and pin 56 is wired to logic ground. When inserting the card to be tested, place the component side of the card up,.
TEST NO-GO push-button switch/indicator	S1	Red lens indicates a detected malfunction (improper time duration) for the edge being tested on the signal selected by the IN/OUT SELECTOR switches S2 and S3. When pressed,

Table 3-1. Card Tester Controls and Indicators (Cont'd)

NAME	REFERENCE DESIGNATION	FUNCTION
		S1 resets all circuits within the Card Tester and performs a new test.
IN/OUT SELECTOR UNITS rotary switch	S2	Used in conjunction with S3 to select the signals to be routed from any one of the 56 pins on the card under test. Switch S2 provides the units digit (0 through 9) for pins 1 through 56.
IN/OUT SELECTOR TENS rotary switch	S3	Used in conjunction with S2 to select the signals to be routed from any one of the 56 pins on the card under test. In addition, S3 provides four self-test switch positions for complete dynamic testing of the major logic circuits comprising the Card Tester. TEST positions 1 through 4 are described in detail below. TEST 1 - Exercises the internal Card Tester oscillator and uses the oscillator output to toggle the self-test flip-flops. TEST 2 - Test 2 further checks the oscillator operation and verifies that the "B" Clock Generator is functioning properly. TEST 3 - Test 3 determines the proper operation of the frame start circuits and checks the "C" Clock Generator. TEST 4 - Test 4 dynamically tests the GO/NO-GO circuits by routing test signal B4 into the edge detector. Tests 1 through 4 require the use of a self-test program card, as explained in paragraph 3-4.
WAVEFORM TEST B rotary switch	S4	Eleven position switch used to select the predetermined bit count at which time a particular transition should

Table 3-1. Card Tester Controls and Indicators (Cont'd)

NAME	REFERENCE DESIGNATION	FUNCTION
		occur in the output waveform being tested. Used in conjunction with S5 to automatically determine the validity of the output signal under test.
WAVEFORM TEST A	S5	Twelve position switch used to select unique transitions of the waveform under test. Test A switch (S5) is used in conjunction with S4 to automatically determine the validity of the output signal under test.
POWER ON/LAMP TEST pushbutton switch/indicator	S6	Blue indicator indicates that primary AC power has been switched on by an IBM tabulating card (containing a program) being inserted into the card reader slot. When pressed, with an IBM card in the card reader slot, a system lamp test function is performed which lights the following lamps: S1 - TEST NO-GO lights red DS1 - TEST GO light green DS2 - TEST INPUT FAULT lights red S6 - POWER ON/LAMP TEST remains illuminated
IN/OUT PIN DIRECT test point	TP1	White test point used to monitor signals at the inputs and outputs of a card under test on the pin selected by the IN/OUT SELECTOR switches, S2 and S3.
IN/OUT PIN IC test point	TP18	White test point used to monitor signals at the inputs and outputs of a card under test on the pin selected by the IN/OUT SELECTOR switches, S2 and S3. The signal levels at TP18 are standard IC levels of from 0 to approximately +3.5 volts.

Table 3-1. Card Tester Controls and Indicators (Cont'd)

NAME	REFERENCE DESIGNATION	FUNCTION
TEST SIGNALS test points	TP2	Monitors test signal +B7
	TP3	Monitors test signal +B6
	TP4	Monitors test signal +B5
	TP5	Monitors test signal +B4
	TP6	Monitors test signal +B3
	TP7	Monitors test signal +B2
	TP8	Monitors test signal +B1
	TP9	Monitors test signal +BO
	TP10	Monitors the internal frame start pulse thus providing a convenient beginning of frame sync pulse for triggering an external oscilloscope.
	TP11	Monitors test signal -C6
	TP12	Monitors test signal +C5
	TP13	Monitors test signal -C4
	TP14	Monitors test signal -C3
	TP15	Monitors test signal -C2
	TP1 6	Monitors test signal -C1
	TP17	Monitors test signal +CO
	TP19	Monitors the output voltage from the ±V power supply
	TP20	Monitors the output voltage from the

Table 3-1. Card Tester Controls and Indicators (Cont'd)

NAME	REFERENCE DESIGNATION	FUNCTION
test points (cont'd)		-V power supply
	TP21	Monitors the output voltage from the +V power supply
	TP22	Monitors the output voltage from the +5V external power supply
	TP23	Monitors the output voltage from the +5V internal power supply e
	TP24	Monitors test signal +S2
	TP25	Monitors test signal +S1
	TP26	Monitors test signal +S0
	TP27	Logic (signal) ground test point.

3-3 SELF TEST PROCEDURES.

Complete and systematic Self Test procedures are provided below to aid the operator/technician in performing functional checks on the Card Tester internal circuits. These tests are structured such that complete and detailed troubleshooting steps have been derived from the individual Self Test steps, providing the technician with fault isolation charts which pin-point internal malfunctions normally encountered in equipments of this type. The information presented in the fault isolation charts, table 5-1, coupled with normal troubleshooting techniques w ill 1 isolate most malfunctions down to the functional area and, in many cases, down to the defective circuit/component. The following paragraphs provide the necessary steps to operate the Card Tester Self Test programs.

3-3.1 AUTOMATIC SELF TEST PROCEDURE. Automatic Self Test of the Card Tester is provided to functionally operate the circuits directly involved in the operation of external printed circuit card testing. This test is automatically initialized via the Automatic Self Test program card, illustrated in figure 4-10, and controlled by the operator from the IN/OUT SELECTOR TENS switch in TEST position 1 through 4. Operate the automatic Self Test according to the following steps:

a. Insert the Automatic Self Test program card into the card reader receiver slot.

Note

If the above step did not produce the required results, refer to fault isolation table 5-2 for corrective action. When executing the following steps, refer to fault isolation table 5-1 for corrective action pertaining to any malfunctions encountered.

b. Rotate the card reader handle to the full CW position and observe the POWER ON indicator, it should be lit.

c. Set the IN/OUT SELECTOR TENS switch to TEST 1. Observe that-the GO indicator is illuminated and the NO-GO and INPUT FAULT indicators are extinguished.

d. Press the NO-GO switch/indicator and observe that the GO indicator extinguishes and the NO-GO indicator lights. Release the NO-GO switch/indicator and observe that the NO-GO indicator extinguishes and the GO indicator lights, as in c above.

e. Place the TENS switch to position TEST 2. Observe that the GO indicator flashes ON and OFF for a period of 4.2 seconds in each state. Initially, it is possible (normal indication) that the NO-GO indicator be illuminated for a period from a few milliseconds (would not light the indicator) to approximately 8.39 seconds. Refer to paragraph 4-11.2 for a detailed explanation of the NO-GO indicator operation.

f. Rotate the TENS switch to TEST 3. Observe that the GO indicator flashes ON and OFF for a period of 4.2 seconds in each state. Initially, when the TENS switch is positioned in TEST 3, it is possible (normal indication) that the NO-GO indicator be illuminated for a period from a few milliseconds (would not be seen by the human eye) to approximately 8.39 seconds. Refer to paragraph 4-11.3 for a detailed explanation of the NO-GO indicator operation in TEST 3 position.

g. Rotate WAVEFORM TEST switch A to position 9.

h. Place WAVEFORM TEST switch B in position 7.

i. Place the TENS switch to TEST position 4 and observe that the GO indicator flashes ON and OFF for a period of 4.2 seconds in each state. Initially, when the TENS switch is placed in the TEST 4 position, it is possible (normal indication) that the NO-GO indicator be illuminated for a period from a few milliseconds (would not be noticed by the human eye) to approximately 8.39 seconds. Refer to paragraph 4-11.4 for a detailed explanation of the NO-GO

indicator operation in TEST position 4.

Note

The above steps complete the Automatic Self Test procedure and indicate that the Card Tester performs as designed for most functional areas within the tester. Further testing is provided by Self Test programs A and B which are presented in the following paragraph.

3-3.2 SELF TEST PROGRAMS "A" AND "B". Programs A and B provide additional testing of the card reader COL and ROW (matrix) circuits, programmable power supplies, and external input wiring. These programs are used to further isolate malfunctions associated with the card reader matrix and Card Tester test signal generator circuits. Programs A and B are executed as follows:

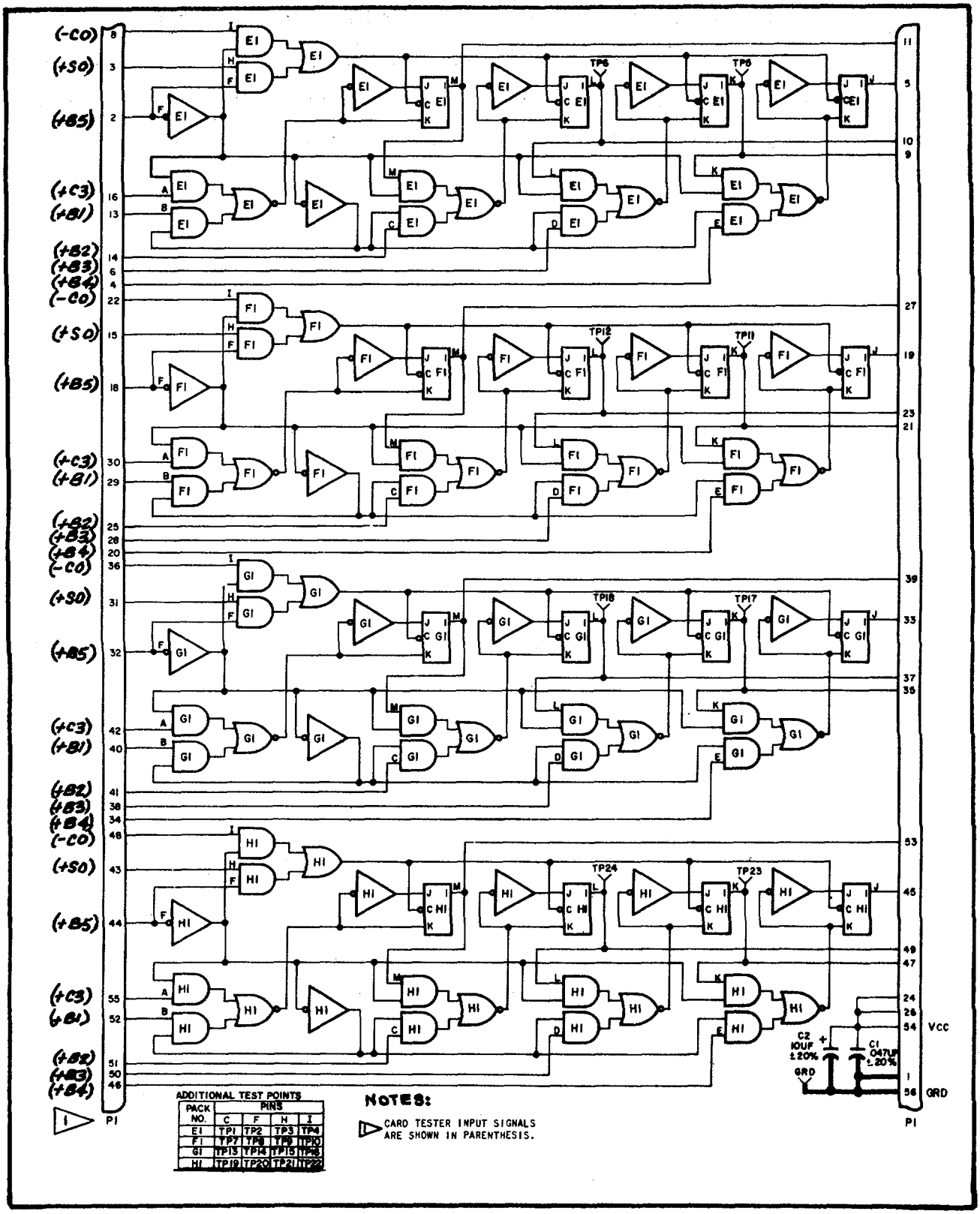
a. Remove the Automatic Self Test program card from the card reader and insert Self Test program card A. (See figure 4-10)

Note

The following steps are referenced to figure 3-2. which illustrates the output waveforms, switch settings, test parameters, ROW assignments and program coding information.

b. Set the TENS and UNITS switches to pin 1. Manipulate the WAVEFORM TEST switches (A and B) through the SWITCH SETTINGS shown in

input (+B1 through +B4) changes states it is loaded into the corresponding flip-flop on the next negative going edge of +SO. As shown in figure 3-19, the flip-flop outputs follow the "B" test signal inputs as long as +B5 remains at a high level. Both the serial shift and parallel load sequence are repeated until the end of the frame.



PACK NO.	PINS C	F	H	I
E1	TP1	TP2	TP3	TP4
F1	TP7	TP8	TP9	TP10
G1	TP13	TP14	TP15	TP16
H1	TP19	TP20	TP21	TP22

Figure 3-18. Programming Example No. 2, Right/Left Shift Register Logic Diagram

figure 3-2 for each pair of switch positions. As each pair of settings are selected, observe that the GO indicator lights.

c. After completion of all combinations of switch settings for the output pin previously selected, set the TENS and UNITS switches to the next output pin number shown in figure 3-2. Again manipulate the WAVEFORM A and B switches through all switch settings listed for the selected output pin number and observe a GO indication for each pair of switch settings.

d. Repeat the above step for all output pins listed in figure 3-2, observing a GO indication for each pair of switch settings.

Note

Output pin 7 (-C6 test signal) contains a # symbol for the third setting of WAVEFORM TEST switch B. This symbol (#) indicates that the GO indicator is extinguished and the NO-GO indicator is illuminated for all twelve positions of switch B.

e. Once all output pin numbers have been checked (as described above), Self Test Program A is completed. Remove the program card from the card reader and continue on with Self Test Program B, described below.

Note

The following steps are referenced to figure 3-3 which illustrates the output waveforms, switch settings, test parameters, ROW assignments and program coding information for Self Test Program B.

f. Set the TENS and UNITS switches to pin 1. Manipulate the WAVEFORM TEST switches (A and B) through the SWITCH SETTINGS shown in figure 3-3 for each pair of switch positions. As each pair of settings are selected, observe that the GO indicator lights.

g. After completion of all combinations of switch settings for the output pin previously selected, set the TENS and UNITS switches to the next output pin number shown in figure 3-3. Again manipulate the WAVEFORM A and B switches through all switch settings listed for the selected output pin number and observe a GO indication for each pair of switch settings.

h. Repeat the above step for all output pins listed in figure 3-3, observing a GO indication for each pair of switch settings.

Note

Output pin 8 (+B7 test signal) contains a # symbol for the third setting of WAVEFORM TEST switch B. This symbol (#) indicates that the GO indicator is extinguished and the NO-GO indicator is illuminated for all twelve positions of switch B.

i. Once all output pin numbers have been checked (as described above), Self Test Program B is completed. Remove the program card from the card reader.

3-4 OPERATING PROCEDURES.

Following is the step-by-step procedure for performing dynamic test analysis on printed circuit cards programmed for the model ICT 102 Card Tester. These instructions pertain to all printed circuit cards; specific instructions peculiar to individual printed circuit cards undergoing tests are listed as notes on the appropriate waveform sheet. Waveform sheets for individual printed

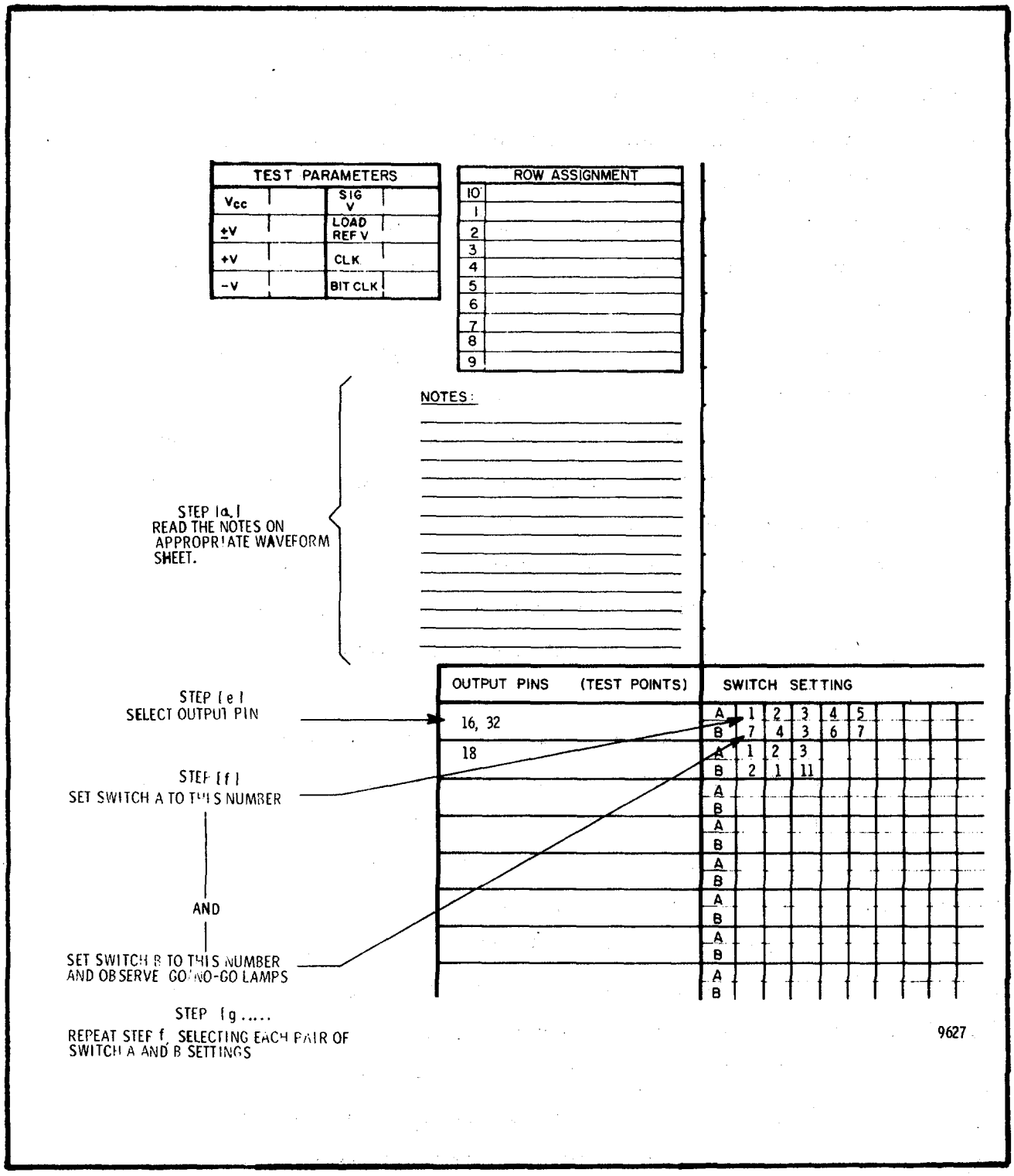


Figure 3-4 Typical Waveform Sheet

circuit cards are located under separate cover, as determined by individual contractural requirements. Before proceeding with any test, the operator should read the notes contained on the waveform sheet and follow any specific instructions > first. In addition the necessary card adapters, card extender cables, and programmable load boards should be inserted in the Card Tester to accomodate the card to be tested. The steps listed below provide the necessary information for successful diagnostic testing of all printed circuit cards programmed for testing with the ICT 102.

a. Refer to the Printed Circuit Card Program manual and locate the appropriate card under test schematic and/or logic diagram and corresponding waveform sheet. On the waveform sheet, locate the notes and follow the instructions pertinent to the operator. Figure 3-4 illustrates the normal location of the notes on a typical waveform sheet.

b. Insert the PC card adapter and/or extender cable (if required) into the CARD IN TEST connector on the front panel of the Card Tester.

c. Insert the printed circuit card to be tested into the card adapter with the component side facing up.

d. Locate-the corresponding card under test program card and insert it into the card reader slot on the front panel of the Card Tester as depicted on the front panel. Push the program card into the card reader slot until there is a noticeable resistance felt against the test card. Move the card reader handle clockwise until it is in the full closed position.

e. Select the output pin to be tested on the front panel IN/OUT SELECTOR switches (S2 and S3). Figure 3-4 shows a typical example of an output pin (pin 16) and its location on the waveform chart.

f. Set WAVEFORM TEST switch A to the first number shown under the SWITCH SETTING heading which corresponds to the selected output pin on the waveform chart. As shown in figure 3-4, the number 1 would be selected by switch A.

g. Place WAVEFORM TEST switch B to the first number adjacent to

SWITCH SETTING B which corresponds to the selected output pin.

h. Observe the three TEST indicators on the front panel and determine the outcome of the circuit being tested. The three possible indications are explained below:

1. GO indicator lights green - circuit being tested checks good for this measurement and the operator should continue with the next step.

2. NO-GO indicator lights red - circuit being tested does not meet the output requirements for the programmed test. Recheck the switch settings to ensure that there has been no operator error and then make the necessary notations on the card in test paper work for follow-up maintenance.

3. INPUT FAULT indicator lights red - one of the inputs to the card under test is short circuited. At this point a qualified technician should be consulted for corrective maintenance procedures applicable to the card under test.

i. Place WAVEFORM TEST switches A and B to the next pair of SWITCH SETTINGS, shown on the waveform chart, and observe the TEST indicators as in the previous step. Continue this procedure until all settings for a given output pin have been carried out and all test indications have been GO.

j. Change both IN/OUT SELECTOR switches to the next output pin number located on the waveform chart either adjacent to the output just tested or, if there is no adjacent number, to the next output pin number directly below the output pin just tested.

k. Place WAVEFORM TEST switches A and B to each pair of corresponding SWITCH SETTING numbers. Continue this procedure until all settings for a given output pin have been carried out and all test indications have been GO. Repeat

j. above and this procedure until all output pins and corresponding SWITCH settings have been tested.

l. Rotate the card reader handle counter-clockwise to the full open

position, remove the program card from the card reader slot and insert the test card into the appropriate plastic card holder.

m. Determine whether or not the card under test requires additional testing using another program test card. If additional testing is required, repeat a through 1 above and this procedure for additional tests. If no further testing is required, remove the tested printed circuit card from the adapter.

3-5 PROGRAMMING AND PREPARATION OF PUNCHED CARDS.

Programming instructions and actual examples of existing programs for ICT 102 Card Tester are delineated in the following paragraphs. Before attempting an actual program, the examples given should be carefully studied as they provide concise models for most situations normally encountered while programming most printed circuit cards. Actual programming approaches to various functional circuits to be tested are not covered in the following paragraphs but, emphasis is placed on the general usage of the test signals available in the Card Tester to provide the programmer with ample information to satisfy most programming approaches. Special attention should be given to the available groups of test signals to fully understand the timing relationships between these groups. A thorough understanding of the "card to be tested" technical characteristics and functional applications is required by the programmer to ensure maximum efficiency of program preparation and utilization of available test parameters. Most functional printed circuit cards are programmed using a single test card which provides a complete dynamic test for the circuits. Some functional circuits require additional test programs to fully exercise all circuitry contained on the printed circuit card. The approach given to these printed circuit cards can only be determined by an individual thoroughly familiar with the functional application of the circuits envolved.

3-5.1 WAVEFORM CHART DESCRIPTION. Initially, programming operations are implemented using one of three waveform charts. The basic waveform chart

(form 738) consists of a full frame of test signals. One-half of a frame of test signals are provided on the 738-1 form and the 738-2 form contains one-quarter frame. All subparagraphs below refer to the form 738 waveform chart, shown in figure 3-5.

3-5.1.1 Test Parameters. Test parameters, under program control, are listed in this table to aid the programmer and technician during initial programming and during printed circuit card testing. Descriptions of these test parameters are given in detail below:

a. Vcc - indicates the required output voltage for the external +5 volt power supply. This power supply is adjustable from +4.5 volts to +5.5 volts and is wired to pin 54 of the CARD IN TEST connector, J3. In addition, the output voltage can be programmed to ROW 10 of the card reader for application to any of the 54 available pin locations on the CARD IN TEST connector. Refer to paragraph 5-3.1 for power supply adjustment procedures.

b. +V - provides the programmed level for the +V power supply output voltage. This level is determined by the programmer (to satisfy particular printed circuit card circuit requirements) and written here to aid programming and printed circuit card troubleshooting.

c. +V - Same as b above except it is the +V power supply output voltage.

d. -V - Same as b above except it is the -V power supply output voltage.

e. SIG V - used to indicate the programmed output signal voltage level of the card under test.

f. LOAD REF V - Lists the programmed load resistor reference voltage applied to the load resistor printed circuit card, 8A, by the programmer.

g. CLK - Four separate internal Card Tester clock rates are available and controlled by programming. These rates include 1usec, 2usec, 32usec, and 16 Msec.

h. BIT CLK - Four individual Bit Counter intervals are under control of the programmer. By controlling the Bit Counter advance rate, many asynchronous circuits can be functionally tested by the Card Tester. Oscillators and single shot circuits fit into the asynchronous circuit category. Under normal conditions the BIT CLK is programmed for 1 usec operation.

3-5.1.2 Row Assignment. The ROW ASSIGNMENT table provides a place for the programmer to record the designated use of each row used by the program. Each of the ten programmable ROWS function in a dual capacity, as determined by the operator. For example, if ROW 10 is selected to route test signal +BO to certain pins on the card under test, +BO would be written adjacent to ROW 10 in the ROW ASSIGNMENT table and so on for all other test signals. This table is provided as an aid to the programmer.

3-5.1.3 Input Pin Waveforms. All available test signals generated in the Card Tester are shown on the waveform chart (under WAVEFORMS) enabling the programmer-to select the necessary signals needed to fully exercise the card under test. In addition to the 15 test signals shown, three signals (+S0, +S1 and +S2) are controlled by the programmer and are individually drawn, as required.

Directly to the left of the test signals, figure 3-5, are two vertical columns containing COL and SIG. COL indicates the card reader column upon which the test signal is located. SIG indicates the test signal designation assigned to each internally generated test signal. To the left of COL there is an area designated INPUT PINS in which the programmer lists the input pins, adjacent to the corresponding test signals applied to these pins. For example, while programming a particular printed circuit card, +B6 is selected to be applied to pin 36 of the card under test. The pin number, 36, would be written under INPUT PINS in the area adjacent to test signal +B6.

3-5.1.4 Output Pin Waveforms. All output pins being tested during a particular test program are listed under the OUTPUT PINS (TEST POINT)

DYNATRONICS TESTAGRAM

DOC NO. SELF TEST PROGRAM "A."
P.C. ASSY
P.C. LOGIC
PROJECT ____ SYSTEM ICT-102
PROGRAMMER
APP / DATE: PROGRAMMER ____ /
GRP LEADER ____ /
DRAFTSMAN

TEST PARAMETERS			
Vcc	+5V	SIG V	0, +5
±V	+6	LOAD REF V	—
+V	+12	CLK	1µs
-V	-12	BIT CLK	OSC

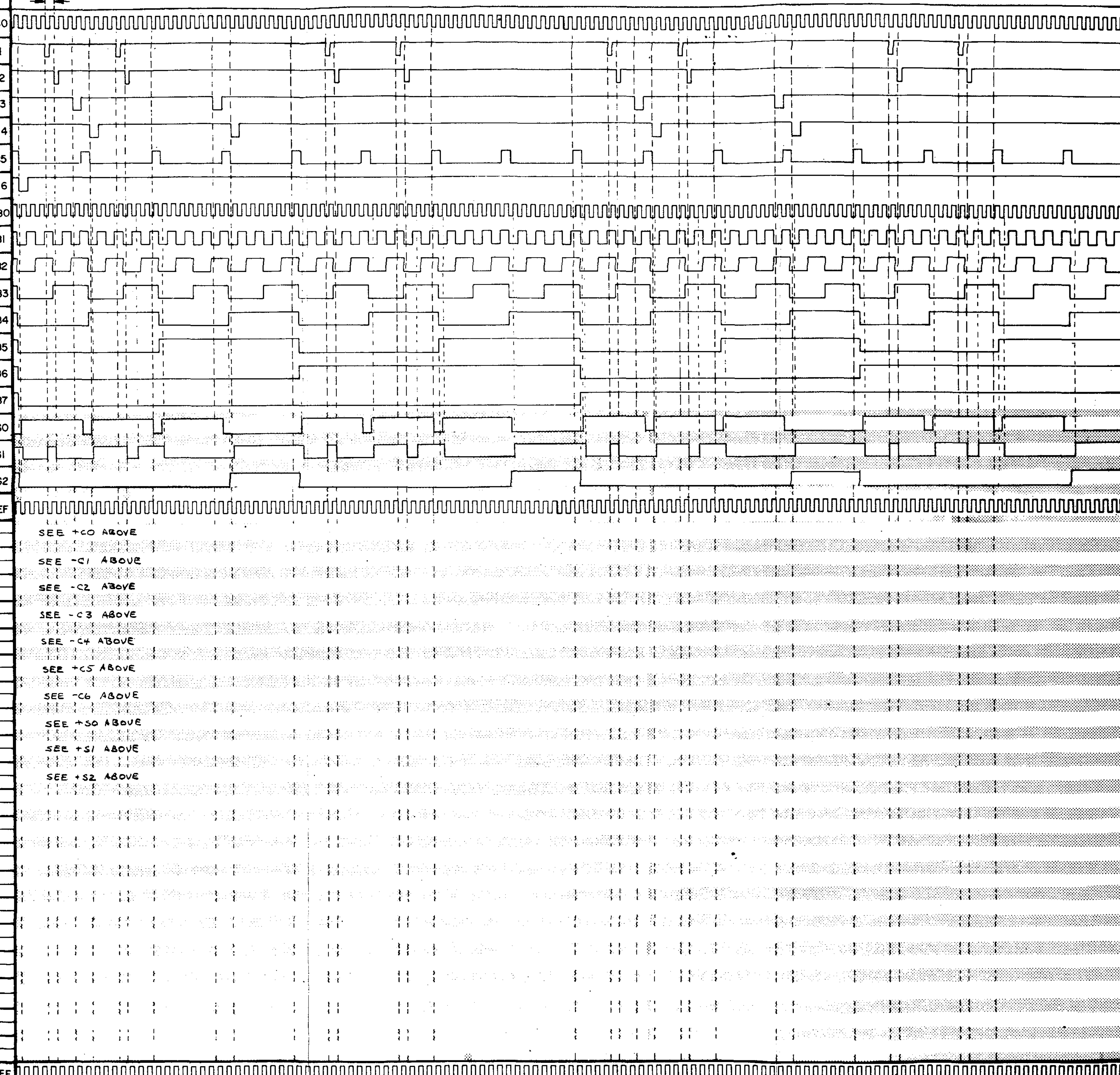
ROW ASSIGNMENT	
10	+S2
1	+C0
2	-C1
3	-C2
4	-C3
5	-C4
6	-C5
7	-C6
8	+S0
9	+S1

COL	PROGRAMMING	
1	1, 11	
2	2, 11	
3	3, 11	
4	4, 11	
5	5, 11	
6	6, 11	
7	7, 11	
8	8, 11	
9	9, 11	
10	10, 11	
11–53		
54	5, 11, 1	
55		
56	9, 8, 5, 4, 3, 10	
57	9, 8, 5, 4, 3	
58		
59	9	
60		
61	10, 1, 2, 3, 4, 5, 8, 9, 1/2	
62	10, 1, 2, 3, 4, 5, 7, 8, 9, 1/2	
63	1	C0
64	1/2, 2	C1
65	1/2, 3	C2
66	4	C3
67	5	C4
68	11, 6	C5
69	7	C6
70	1/2	B0
71		B1
72		B2
73		B3
74	1/2, 11	B4
75	11	B5
76		B6
77		B7
78	8	S0
79	9, 1/2	S1
80	10	S2

NOTES:
1. # DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO.

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
	+C0 REF	
	+B0 REF	

WAVEFORMS



OUTPUT PINS (TEST POINTS)	SWITCH SETTING							
1 (+C0)	A	1	2	3				
	B	3	5	7				
2 (-C1)	A	1	2	3	4	5		
	B	4	6	3	5	11		
3 (-C2)	A	1	2	3	4	5		
	B	8	10	7	9	4		
4 (-C3)	A	1	2	3	4	5		
	B	5	9	3	7	8		
5 (-C4)	A	1	2	3	4	5		
	B	2	6	11	4	5		
6 (+C5)	A	1	2	3				
	B	3	9	2				
7 (-C6)	A	1	2	3				
	B	3	7	#				
8 (+S0)	A	1	2	3	4	5	6	7
	B	3	9	2	8	!	7	10
9 (+S1)	A	1	2	3	4			
	B	4	4	8	3			
10 (+S2)	A	1	2	3				
	B	2	10	9				

Figure 3-2. Self Test Program A

DYNATRONICS TESTAGRAM

DOC NO. SELF TEST PROGRAM "B"
P.C. ASSY.
P.C. LOGIC.
PROJECT _____ SYSTEM ICT-136
PROGRAMMER
APP / DATE: PROGRAMMER / /
GRP LEADER / /
DRAFTSMAN

TEST PARAMETERS			
V_{cc}	+5V	SIG V	+18, -6
±V	-10	LOAD REF V	—
+V	1 - .8	CLK	1uS
-V	-6	BIT CLK	0 SC

ROW ASSIGNMENT	
10	
1	EXT IN
2	B1
3	B2
4	B3
5	B4
6	B5
7	B6
8	B7
9	B0

COL PROGRAMMING

NOTES:
1. # DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO.

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
1 (+B0)	A 1 2 3 / B 2 4 6
2 (+B1)	A 1 2 3 / B 2 6 10
3 (+B2)	A 1 2 3 / B 2 10 7
4 (+B3)	A 1 2 3 / B 2 7 1
5 (+B4)	A 1 2 3 / B 2 1 11
6 (+B5)	A 1 2 3 / B 2 11 9
7 (+B6)	A 1 2 3 / B 2 9 5
8 (+B7)	A 1 2 3 / B 2 5 #
9 (EXT IN)	

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

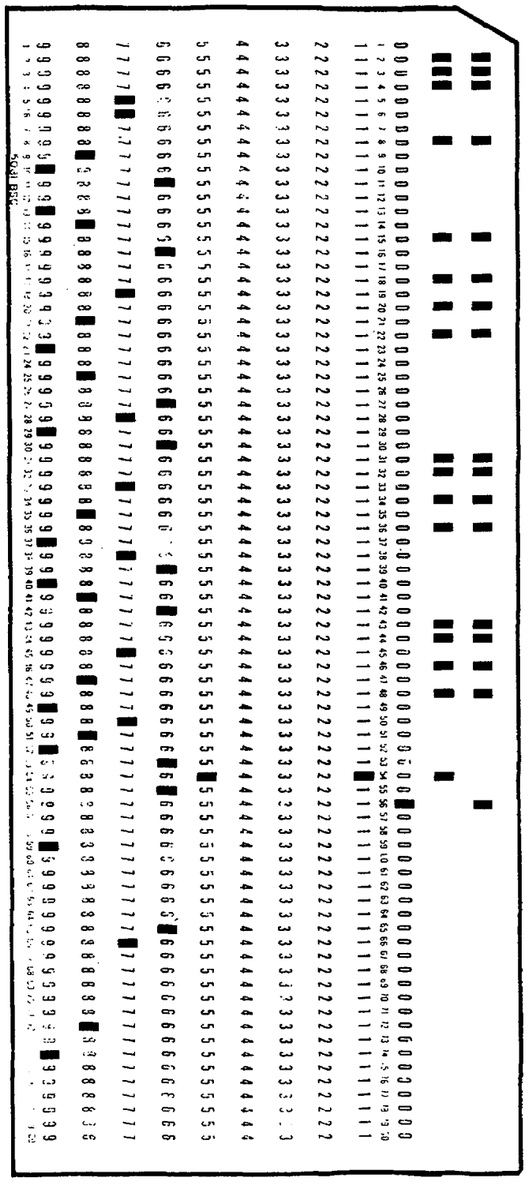
WAVEFORMS

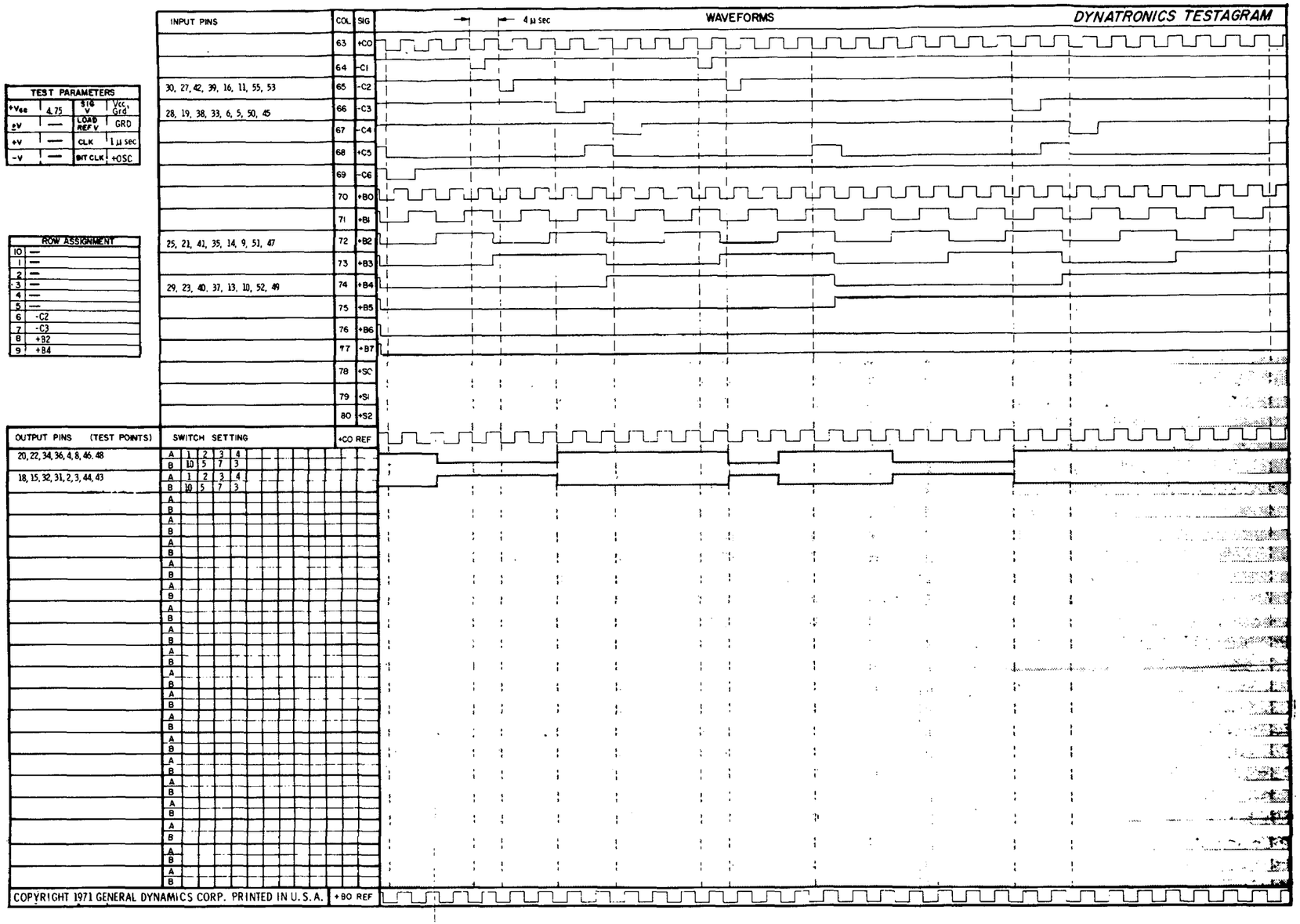
+C0 REF

SEE +B0 ABOVE
SEE +B1 ABOVE
SEE +B2 ABOVE
SEE +B3 ABOVE
SEE +B4 ABOVE
SEE +B5 ABOVE
SEE +B6 ABOVE
SEE +B7 ABOVE
+5V

+B0 REF

Figure 3-3. Self Test Program B





P.C. Assembly 08-890508-1

P.C. Assembly 08-890508-1
Figure 3-17. Programming Example No.1

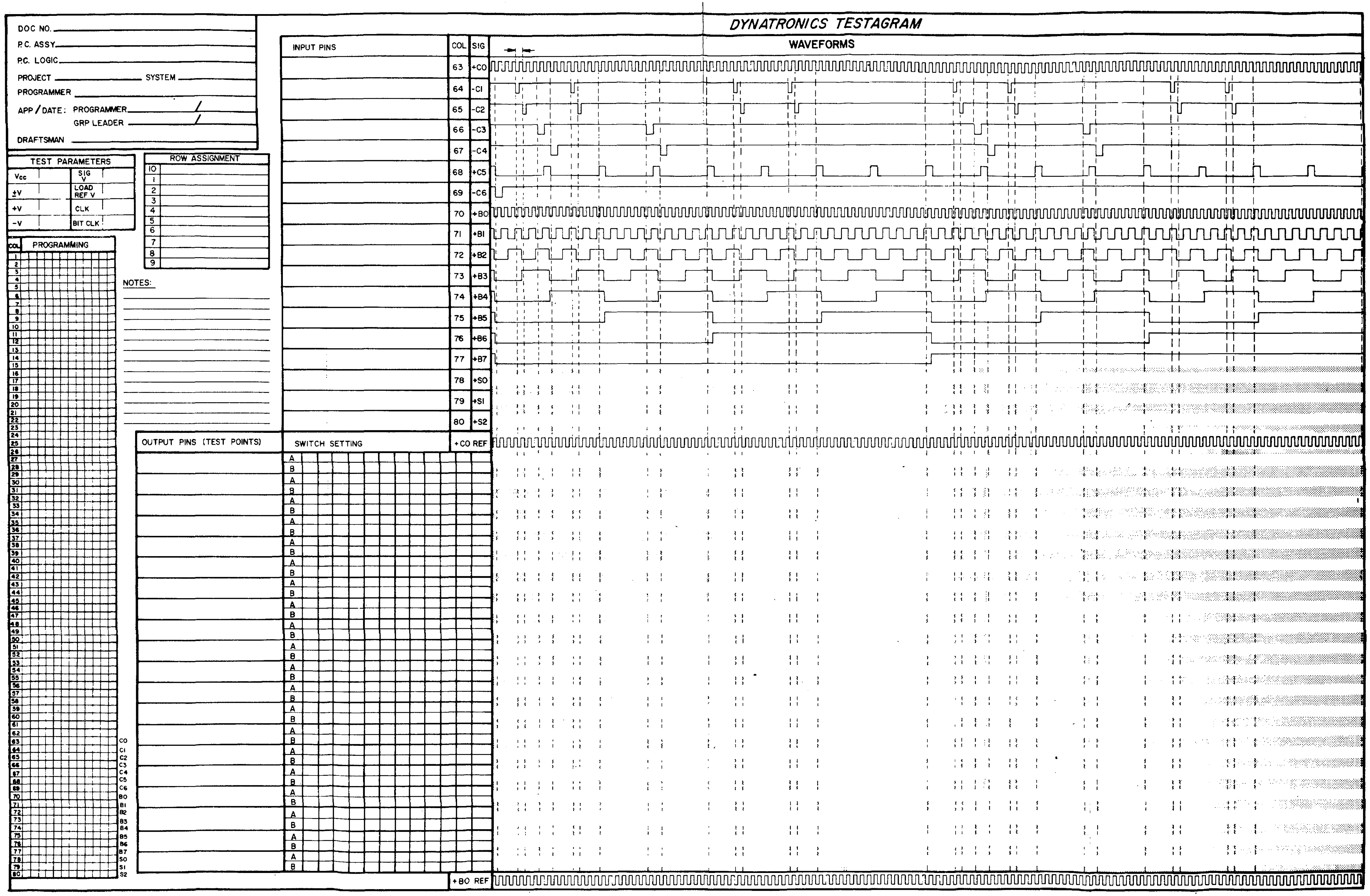


Figure 3-5. Programming Waveform Chart

heading located in the lower left hand side of figure 3-5. Corresponding output signals are drawn adjacent to the pin number location, directly below the input waveform test signals. Vertical dashed lines have been extended down through the WAVEFORM area on the waveform chart enabling the programmer to accurately record the associated output waveforms.

Note

Accurate reproduction of output pin waveforms must be stressed, to allow maintenance personnel to reliably perform troubleshooting and maintenance techniques on malfunctioning printed circuit cards.

In many cases functional cards (of the building block variety) contain several identical stages. In this situation the programmer should strive to program these circuits identically thus, providing a single output waveform applicable to several output pins. In this manner -the output waveform need only be drawn once and all identical output pins are listed adjacent to the single output waveform and are tested in the same manner.

3-5.1.5 Switch Settings. To the left of the output pin waveform locations is an area designated SWITCH SETTINGS, figure 3-5. This area is used to list the steps required to fully test each output circuit. The switch settings are determined after the program is written and verified. Switch setting A corresponds to a given edge in the output signal. A maximum of twelve edges are selected by switch A. Switch setting B relates the expected edge (transition) location within the Card Tester frame. Edge locations are pin -pointed by an 11: 1 counter (Bit Counter) which operates at the rate faster than the highest available rate from the test signals. Once a program is

written, follow the steps listed below to determine the necessary switch settings for switch A and B.

a. For a given output signal, determine the number of edges required to ascertain that the circuit being tested is fully exercised. This number can be any value from one through 12, typically 4 or 5.

1. At what point does the output signal become repetitious?

2. If, during a complete frame, the number of transitions is less than twelve, insert a # symbol in the last switch setting location to indicate that this position is checked for all 11 positions of switch B to indicate a NO-GO condition. In this case the Card Tester checks the output signal of the card under test for additional transitions beyond the last expected transition. When the # symbol is used for any of the switch settings, a note to that effect should be inserted in the NOTES on the waveform chart.

3. Identical but inverted signals can share the same output signal waveform if the inverted output is designated by an asterisk (*) adjacent to the inverted output pin number. If used, a note should appear in the NOTES on the waveform chart indicating its usage.

b. Denote the number of edges in the appropriate output signal by inserting sequential numbers 1 through X (where X equals the required number) in the squares adjacent to the output signal under SWITCH SETTING A.

c. With the card to be tested inserted into the test connector (J3); the program card correctly inserted into the card reader; and the proper output pin selected on the IN/OUT SELECTOR switches, set switch A to the first edge (number 1).

d. Rotate switch B (halting rotation at each position momentarily) from position 1 through position 11 until the GO indicator illuminates.

e. Record the position of switch B (determined by the GO indication noted in the step above) in the block next to SWITCH B, under the appropriate SWITCH A entry (number 1 in this case).

f. Increase the setting of switch A by one.

g. Rotate switch B (momentarily halting at each switch setting) from Position 1 through position 11 until the GO indicator illuminates. Record the position of switch B in the block next to SWITCH B under the appropriate switch A entry. Repeat f above and this procedure until all switch settings for a given output have been determined.

h. Repeat c through g above for all output pin numbers verifying that all like outputs have identical switch settings.

3-5.1.6 80 X 12 Matrix. An 80 X 12 : matrix (table) is located in the lower left hand corner of the waveform chart for recording the necessary programming information required in the final punched IBM tabulating card. As the programming is prepared for a given printed circuit card, coding numbers are inserted into the table to keep a record of the program. Once programming operations are complete, the table is used either by a key punch operator or by the programmer, using a hand operated IBM card punch, to prepare the punched program card. Any changes to the program should be recorded in the table, to ensure that a uniform record is available for each program.

3-5.2 PRINTED CIRCUIT CARD PROGRAMMING PROCEDURE. Utilizing the Card Tester for testing printed circuit cards requires an understanding of the programming fundamentals, basic theory of operation and a thorough knowlege of the printed circuit card family being tested. Testing concept and approach given to a particular programming problem can only be discussed in general terms, as each programmer will make decisions based on personal experience and knowledge. Following are several general concepts to be taken into consideration prior to actual programming:

a. Isolate identical circuits within the same card and use the same test for these circuits, to avoid unnecessary programming and waveform drawings.

b. Select a waveform chart (full, half, or quarter frame) with the largest duration between edges to ease drawing repetitive output waveforms.

c. Where possible select test signals to provide maximum input testing capability throughout the same printed circuit card thus, reducing the number of different ROWS used.

d. Determine the use of the card to be tested and duplicate its function where possible.

e. Check the printed circuit card technical characteristics and keep minimum and maximum ratings in mind when programming the Card Tester test parameters.

f. Carefully analyze the programmed printed circuit card outputs and ensure that each output tested conforms to the expected output thus, eliminate documenting a malfunctioning printed circuit card.

g. Determine the loading characteristics of the printed circuit cards being tested and ensure that the programmable load resistor cards in the Card Tester match the card under test requirements.

3-5.3 CARD READER STRUCTURE. The internal card reader is a self contained Hollerith 12 X 80 column tabulating card reader which utilizes a manually operated card insertion mechanism. The reading of the card is accomplished by the contact springs of the spring and block assembly, that align in the program card holes, making electrical contact with the corresponding strip on the printed circuit board when the unit is fully closed. Basically the card reader functions as a multi-pole multi-position switch whereby all circuits, as selected by the wiring, are connected simultaneously. The double wiping action of the contact switches provides a cleaning action on the contact points each time the tabulating card is inserted thus, ensuring a positive contact each time a card is read. Refer to figure 3-6 which illustrates the contact spring, IBM card and printed circuit board arrangement.

The model 2981A card reader (modified per Dynatronics specification 04-001196, see parts list) is manufactured by AMP Incorporated to provide a card

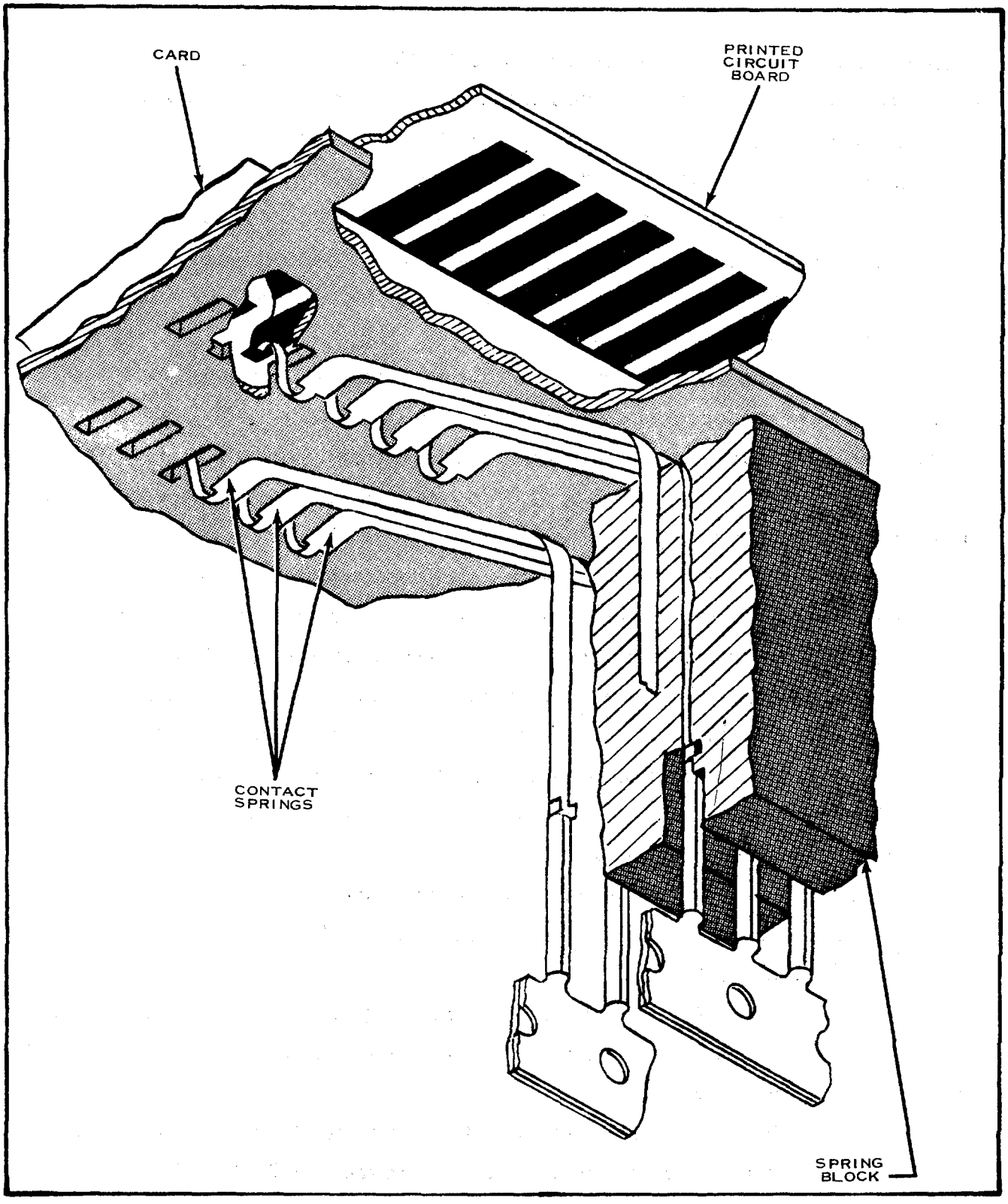


Figure 3-6. Typical Contact Spring, IBM Card and PC Board Arrangement

reader which conforms to EIA Standard RS 292, Media I. All instructions pertaining to the operation and maintenance of this unit are contained in this manual. Simplicity of design permits easy disassembly for periodic maintenance and repair, as delineated in section V. The spring and block assembly is factory assembled in special manufacturing fixtures and CANNOT be disassembled. In the event of broken contact springs, or other damage beyond repair, the complete assembly must be replaced. All wiring, including busses and jumpers, is shown on drawings D3006 and D3007, section VII.

All program control and signal routing operations are accomplished through the card reader matrix. In general, the 12 ROW by 80 COL matrix (figure 3-7) is divided into three main groups to control signal routing, power supply programming and internal Card Tester control functions. Group 1 consists of 54 pins connected to the CARD IN TEST connector (J3) on the front panel of the Card Tester. Any 10 of the 18 internally generated test signals and power supply outputs can be connected to any or all of 54 pins on the 56 pin test connector. Group 2 consists of an area dedicated to program control parameters for the Card Tester and group 3 provides the test signal routing and distribution area. Rows 1 through 10 in the test connector area (group 1) are used to route power and test signals to the card under test, via the CARD IN TEST connector. Rows 11 and 12 provide programmable loading resistors for the circuits under test. Rows 1 through 10 are described below:

a. ROW 1 - Driven by any test signal connected to line driver number one or used to route an external input (connected via J1 or J2 on the front panel) into the card under test.

b. ROW 2 - Used either to route any programmed test signal from line driver number two or the output from the +V power supply to any pin the CARD IN TEST connector on the front panel.

c. ROW 3 - Routes either the output from the +V power supply or the output from line driver number three to any pin on the CARD IN TEST connector on the front panel.

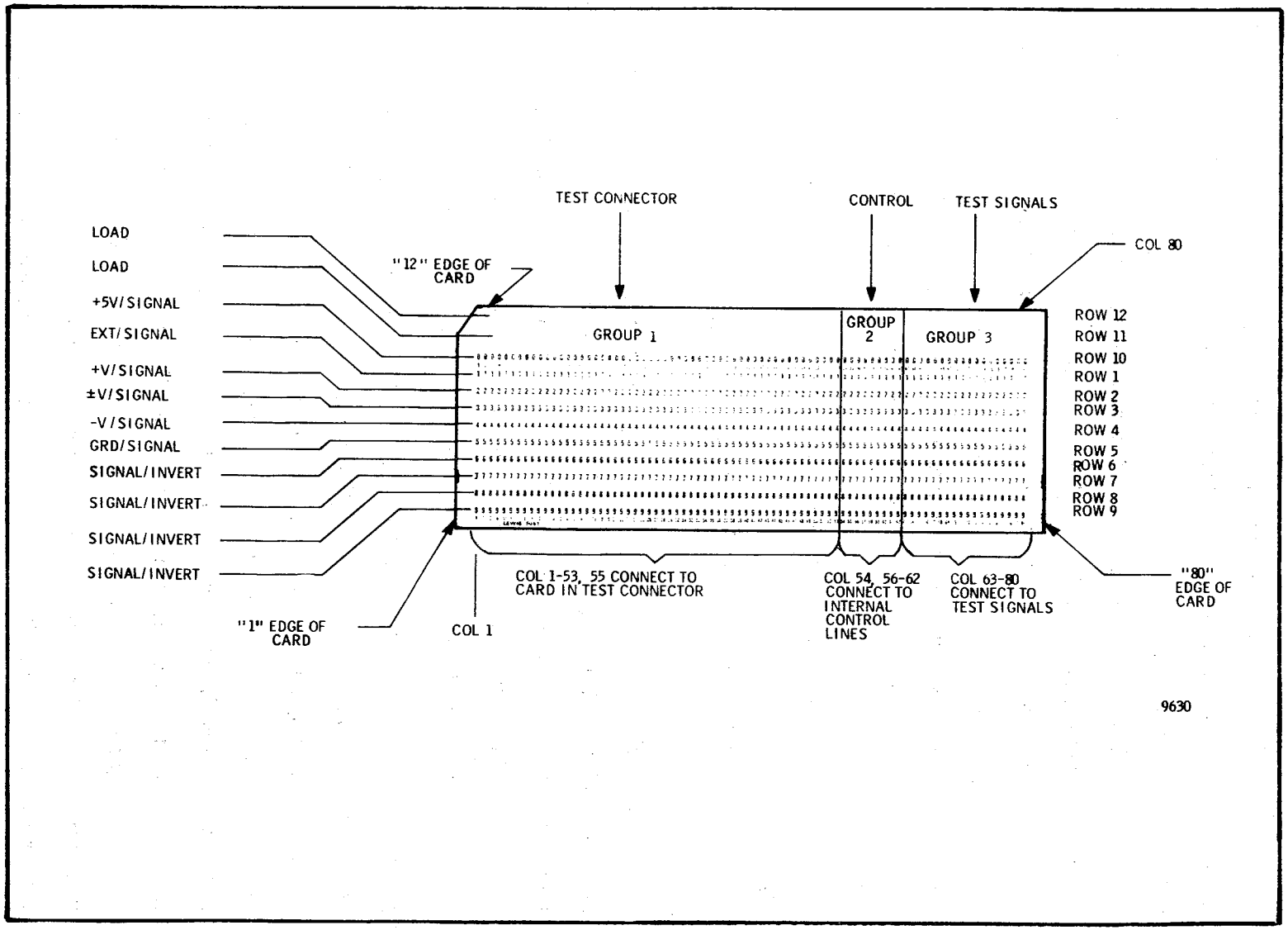


Figure 3-7. Card Reader 12 X 80 Matrix Layout

d. ROW 4 Routes either the output voltage from the -V power supply or the output from line driver number four to any pin in the CARD ON TEST connector on the front panel.

e. ROW 5 Routes either power ground or the output from line driver number 5 to any pin on the CARD IN TEST connector on the front panel.

f. ROW 6 Routes either the true or complement form of any test signal applied to line driver number six to any pin on the CARD IN TEST connector on the front panel. The test signal may be inverted.

g. ROW 7 Same as ROW 6 above except uses line driver number seven.

h. ROW 8 Same as ROW 6 above except uses line driver number eight.

i. ROW 9 Same as ROW 6 above except uses line driver number nine.

j. ROW 10 Provides a connecting path from either line driver number 10 (which buffers all test signals from COL 63-80) or the +5 VDC EXT power supply output to any pin on the CARD IN TEST connector on the front panel.

Inputs to the line drivers described above are determined by the programmer and instructions for their use are described in paragraph 3-5. 7.

3-5.4 POWER SUPPLY PROGRAMMING. The Card Tester contains three programmable power supplies (+V, -V, and +V) and a logic power supply (+5V EXT), any or all of which may be used to supply voltages to the card under test. Each of the +V, -V, and +V power supplies can be independently programmed to 26. 1 volts DC in 100 millivolt steps. ' Two of the programmable power supplies provide a positive or negative output voltage (+V and -V) which can be applied to any of 54 pins on the CARD IN TEST connector, via ROW 2 and ROW 4 respectively. If either ROW 2 or ROW 4 are used to supply a voltage to the card under test, that ROW(S) CANNOT be used for applying a test signal to the card under test. The third programmable power supply (LV), like the first two, can be programmed in 100 millivolt steps to 26. 1 volts DC (except 1 volt is the

minimum output). The output polarity of the +V power supply can be programmed for either a positive or negative output voltage. Also, the +V supply can provide either sink or source current. The +V power supply output voltage is applied to any of the 54 pins on the CARD IN TEST connector via ROW 3 which, when used for supplying a voltage to the card under test CANNOT be used for routing a test signal to the card being tested.

The +5V EXT power supply is intended for use as a logic power supply and is manually adjustable (from the rear panel) from +4. 5 volts to +5. 5 volts DC. Its output is routed to pin 54 in the CARD IN TEST connector and in addition, can be applied to any of the 54 programmable pins in the test connector on ROW 10 of the card reader matrix. If ROW 10 is used to supply the +5V EXT power supply output to additional pins, it CANNOT be used to route a test signal to the card under test.

Both the +V and -V programmable power supply output voltages are controlled by eight binary weighted inputs to provide the output range from 500 millivolts to 26. 1 volts. These input control lines are located in group 2 (see figure 3-7) of the card reader matrix and table 3-2 below lists the programmed output voltage change for each of the eight inputs.

Each of the eight inputs to the power supply provides a discrete change in the overall power supply output. For example, programming VPI causes the output voltage to change by 100 millivolts, VP2 adds 200 millivolts, and so on. Both the -V and +V power supplies are adjusted for a zero scale (none of the eight inputs programmed) of 500 millivolts. As each input is programmed, its output voltage value is added to the Zero Scale voltage value to determine the power supply output voltage. Power Supply $\pm$V cannot be programmed below 1. 0 volt. All programmable input lines to the $\pm$V power supply cause the same Delta change as the +V and -V power supplies.

Table 3-2. Programmable Power Supply Input/Output Delta

DISCRETE PROGRAMMING VP1 THROUGH VP8	VOLTAGE	DELTA (V)
FULL SCALE	26.1	
VP8	13.3	12.8
VP7	6.9	6.4
VP6	3.7	3.2
VP5	2.1	1.6
VP4	1.3	0.8
VP3	0.9	0.4
VP2	0.7	0.2
VP1	0.6	0.1
ZERO SCALE	0.5	

Minimum voltage to which the $\pm$V supply may be programmed is 1.0V.

Note

Table 3-2 provides programming information for each of the three programmable power supplies. The $\pm$V power supply should not be programmed below 1. 0 volt for either polarity output voltage.

3-5.4.1 Programming Instructions For +V Power Supply. The +V power supply can be programmed over a range of 500 millivolts to +26. 1 volts. Once programmed, the +V power supply output voltage is applied to ROW 2 and can then be programmed to any one or combination of pins in the CARD IN TEST connector . The following steps should be followed when programming the +V power supply.

a. Determine the output voltage desired (refer to table 3-2) and punch the necessary holes in the test card according to the following chart.

VP INPUT	ROW/COL LOCATION	
	ROW	COL
VP1	9	56
VP2	8	56
VP3	7	56
VP4	6	56
VP5	5	56
VP6	4	56
VP7	3	56
VP8	2	56

b. Apply the output from the +V power supply to ROW 2 by punching a hole in ROW 2, COL 59. Ensure that the following holes are not programmed:

1. ROW 2, COL 61

2. ROW 2, COL 62

c. Route the +V power supply output to any pin in the CARD IN TEST connector by punching ROW 2 in the column (COL) corresponding to the desired pin location. For example, punching a 2 in COL 4, 5, 37 and 42 applies the +V power supply output voltage to pins 4, 5, 37 and 42 in the CARD IN TEST connector. If an adapter is used, refer to the appropriate card adapter cross reference table.

3-5.4.2 Programming Instructions for -V Power Supply. The -V power supply can be programmed over a range of -500 millivolts to -26. 1 volts. Once programmed, the -V power supply output voltage is applied to ROW 4 and can then be programmed to any one or combination of pins in the CARD IN TEST connector. The following steps should be followed when programming the -V power supply.

a. Determine the output voltage desired (refer to table 3-2) and punch the necessary holes in the test card according to the following chart.

VP INPUT	ROW/COL LOCATION	
	ROW	COL
VP1	9	57
VP2	8	57
VP3	7	57
VP4	6	57
VP5	5	57
VP6	4	57
VP7	3	57
VP8	2	57

b. Apply the output from the -V power supply to ROW 4 by punching a hole in ROW 4, COL 58. Ensure that the following holes are not programmed:

1. ROW 4, COL 61

2. ROW 4, COL 62

c. Route the -V power supply output to any pin in the CARD IN TEST connector by punching ROW 4 in the column (COL) corresponding to the desired pin location. For example, punching a 4 in COL 4, 5, 37, and 42 applies the -V power supply output voltage to pins 4, 5, 37, and 42 in the CARD IN TEST connector. If an adapter is used, refer to the appropriate card adapter cross reference table.

3-5.4.3 Programming Instructions For +V Power Supply. The $\pm$V power supply is programmed in the same manner as the +V and -V power supplies with the additional steps necessary to determine the power supply output polarity. Also, the $\pm$V supply may not be programmed for an output voltage of less than 1. 0V. Once the output voltage is determined and the polarity is programmed, the output voltage is applied to ROW 3 and then to any pin or combination of pins in the CARD IN TEST connector. Follow the steps given below:

a. Determine the absolute value of the output voltage desired, as listed in table 3-2, and punch the necessary holes in the program test card

according to the following chart. DO NOT program the +V power supply for an output voltage less than 1. 0 volt (either polarity).

VP INPUT	ROW/COL LOCATION	
	ROW	COL
VP1	9	62
VP2	8	62
'VP3	7	62
VP4	6	62
VP5	9	61
VP6	8	61
VP7	7	61
VP8	6	61

b. Determine the output voltage polarity and make the necessary hole punches in the program test card (tabulating card) for the appropriate polarity as listed below:

1. POSITIVE POLARITY - Punch the following:

ROW	COL
12	61
12	62

2. NEGATIVE POLARITY - Punch the following:

ROW	COL
11	61
11	62

c. Apply the $\pm$V power supply output to ROW 3 by punching a hole in ROW 3, COL 58. Ensure that the following holes <u>are not</u> programmed when ROW 3 is utilized for the $\pm$V power supply output.

1. ROW 3, COL 61
2. ROW 3, COL 62

d. Route the $\pm$V power supply output to any pin in the CARD IN TEST connector by punching ROW 3 in the column (COL) corresponding to the desired

pin location. For example, punching a 3 in columns 7,32, 47 and 55 applies the programmed +V power supply output to pins 7,32, 47 and 55 of the CARD IN TEST connector. If an adapter is used, refer to the appropriate card adapter cross reference table for the correct pin number correlation between connectors.

3-5.4.4 Programming Instructions for +5V EXT Power Supply. The output voltage from the +5V EXT power supply can be routed to any or all pins in the CARD IN TEST connector, in addition to being available on pin 54 of the connector. The following steps provide the required information necessary to program this power supply:

a. Locate R10 on the rear of the Card Tester chassis and adjust the +5V EXT power supply output voltage (if required) to the desired value (adjustable through the range from +4. 5V to +5. 5V). The output voltage can be monitored from TP22 (+5 EXT) on the front panel.

b. Route the output voltage to ROW 10 by punching ROW 10, COL 54. Ensure that the following card reader matrix locations are not programmed when ROW 10 is utilized for the +5V EXT power supply output.

1. ROW 10, COL 61

2. ROW 10, COL 62

c. Route the +5V EXT power supply output to any pin in the CARD IN TEST connector by punching a 10 in the column (COL) corresponding to the desired pin location. For example, punching a 10 in columns 2, 7, 34, and 48 applies the output voltage from the +5V EXT power supply to pins 2, 7, 34, and 48 of the CARD IN TEST connector. If an adapter is used, refer to the appropriate card adapter cross reference table for the correct correlation between connector pin numbers.

3-5.5 PROGRAMMABLE DRIVER OUTPUT LEVEL PROGRAMMING. Any 10 of the test signals generated in the Card Tester are available for routing to any or all of 54 pins in the CARD IN TEST connector. These signals are routed through any number or combination of programmable line drivers, as determined by the

programmer, to provide test signals at voltage levels compatible with the circuits on the card under test. Each of the 18 test signals can be programmed into any one (or all) of the ten available line drivers. Each line driver is associated with an individual ROW in the card reader matrix and each of the 10 ROWS will drive any of the 54 pins in the CARD IN TEST connector. Test signals are connected to the inputs of the line drivers via group 3 (see figure 3-7) of the card reader matrix. The line driver output signal level is determined by the driver reference voltages (+DVR REF and -DVR REF) connected to the drivers through the card reader matrix (group 2). These reference voltages provide either a unipolar output signal up to approximately 26 volts (positive or negative) amplitude or a bi-polar output signal with a maximum amplitude of 30 volts peak -to-peak. Line driver output voltage levels are determined by the programmed output voltage from the selected power supplies, as shown in table 3-3. The following steps are taken to program the line drivers:

a. Determine the high and low limits of the test signals required to exercise the circuits contained on the card to be tested. Refer to table 3-3 and locate the available power supply output voltages which satisfy these conditions. Power supply programming instructions are delineated in paragraph 3-5.4.

CAUTION

DO NOT exceed 30 volts difference between the (+) and (-) DVR REF voltages input into the line drivers. In addition, if the driver reference voltages are programmed to provide a peak-to-peak signal swing of 20 volts or greater and, if the Card Tester test rate is programmed for 1 microsecond (COL 54, ROW 5) then, DO NOT program test signals BO or CO (or an "S" test signal of equal switching rate) into a driver. In either case the drivers may be damaged. In the latter case, exceeding a 2 microsecond switching time duty cycle causes excessive heating of the drive output transistors.

Table 3-3. Line Driver Reference Voltage Programming.

CONNECT		+DVR REF EQUALS	CONNECT		-DVR REF EQUALS
COL	ROW		COL	ROW	
54	11	+5V	56	10	GRD
56	11	GRD	57	10	-V
58	11	±V	58	10	±V
59	11	+V			

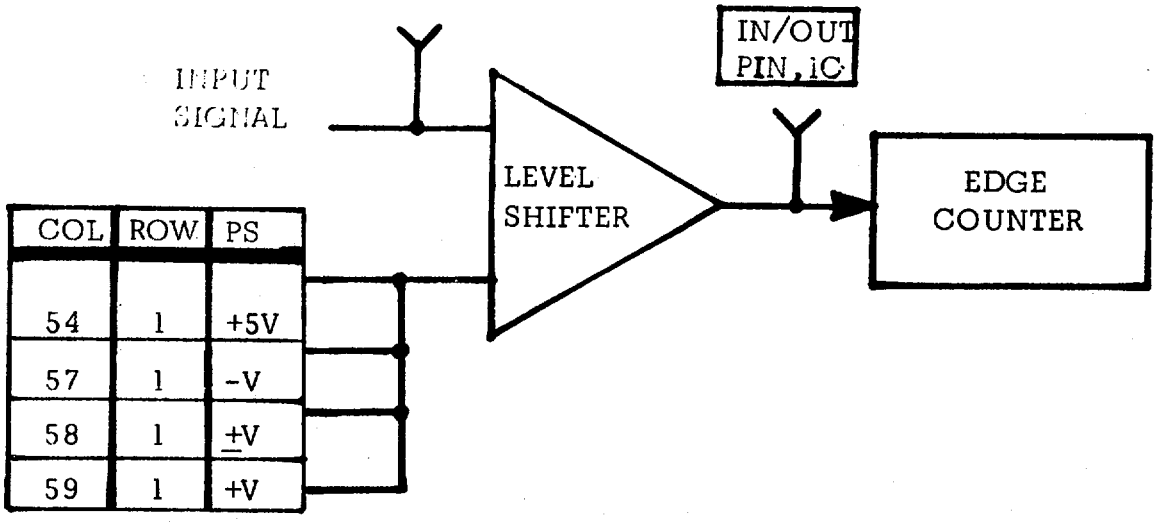
Note

When programming +DVR REF and -DVR REF only connect one of the DC voltages in each of ROWS 10 and 11 and ensure that the total difference does not exceed 30 VDC.

b. Make the necessary punches to satisfy the card in test signal requirements as determined from table 3-3.

c. Record the programmed signal level in the TEST PARAMETERS table (SIG V) of the waveform chart.

3-5.6 LEVEL SHIFTER THRESHOLD PROGRAMMING. The level shifter is programmed such that it will slice the output signal under test at approximately mid-range of the peak-to-peak signal voltage level. Typically, one of the Card Tester power supply output voltages will satisfy the level shifter voltage requirements in that it will slice at approximately one-half the value of the power supply voltage connected to the level shifter input via the card reader matrix. For example, programming the level shifter with T+V (COL 54, ROW 1) causes the level shifter to slice the signal under test at approximately +2. 5V.



In special cases where level shifters or line drivers are being tested, up to four Card Tester power supply voltages can be utilized to provide an adequate Card Tester level shifter threshold voltage. When using more than one power supply voltage to provide a unique threshold voltage, calculate the threshold voltage from the formulas given below:

V_t -=1/2 V_1

Vt = 6/13 (V_1 + V_2)

Vt = 6/14 (V_1 + V_2 + V)

Vt = 6/15 (V_1 + V_2 + $_{V3}$ +V_4

WHERE:

V_t = Threshold Voltage

V_1 = Any one power supply output voltage.

V_2 = Any second power supply output voltage.

V_3 = Any third power supply output voltage.

V_4 = Any fourth power supply output voltage.

With no power supply voltages programmed into the level shifter the threshold voltage equals OV.

3-5.7 TEST SIGNAL ROW USAGE. Eighteen test signals, shown in figure 3-3, are generated by the Card Tester for testing applications related to external printed circuit cards. Each of these test signals is available on individual columns within group 3, see figure 3-7, of the card reader matrix. Table 3-4 lists the 18 test signals and their related locations within the card reader matrix.

Table 3-4. Test Signals Column Assignments

TEST SIGNAL	COLUMN	TEST SIGNAL	COLUMN
+CO	63	+B3	73
-C1	64	+B4	74
-C2	65	+B5	75
-C3	66	+B6	76
-C4	67	+B7	77
+C5	68	+S0	78
-C6	69	+S1	79
+B0	70	+S2	80
+B1	71		
+B2	72		

To apply a desired test signal to a given pin in the CARD IN TEST connector, the programmer must program the following:

1. Input the test signal to a card reader ROW.
2. Connect the programmable line driver output to the selected ROW (Rows 10, 1-5 only).
3. Connect the selected ROW containing the desired test signal to the required CARD IN TEST pin (s).

The necessary steps required to perform the above programming operations are described below:

ROWS 1 through 5 and 10

a. Connect a test signal to a line driver by punching the selected ROW number (1 through 5 or 10) in the COL associated with the test signal, as listed in table 3-4. For example, to connect test signal +CO to ROW 2 simply punch ROW 2, COL 63.

b. Connect the output of the line driver, chosen in the step above, to the card reader ROW by punching the selected ROW number in COLS 61 and 62. As in the above example where ROW 2 is used, punch ROW 2, COL 61 and ROW 2, COL 62.

c. Connect the test signal to the CARD IN TEST connector pin (s) by punching the appropriate ROW number in the COL associated with the selected pin(s). As in the above example, a 2 (indicating ROW 2) would be punched in the columns associated with the selected pin(s).

ROWS 6 through 9

a. Connect a test signal to a line driver by punching the selected ROW number (6 through 9) in the COL associated with the test signal, as listed in table 3-4. For example, to connect test signal +CO to ROW 2 simply punch ROW 2, COL 63.

b. Connect the test signal to the CARD IN TEST connector pin(s) by punching the appropriate ROW number in the COL associated with the selected pin(s).

Inverted Test Signals (ROWS 6 through 9)

To invert any test signal applied to ROW drivers 6, 7, 8, or 9, program the desired ROW number in COL 54 as shown below:

ROW	COL	INVERTS
6	54	Test signal applied to line driver six
7	54	Test signal applied to line driver seven
8	54	Test signal applied to line driver eight
9	54	Test signal applied to line driver nine

All ROWS in the card reader are dual purpose and care must be exercised when selecting a particular ROW to avoid utilizing the same ROW for both functions. A list of each ROW and its programmable function is provided in table 3-5.

Table 3-5. Card Reader ROW Usage

ROW USAGE (COL 1-53 and 55)										
SIGNAL SOURCE	1	2.	3	4	5	6	7	8	9	10
Programmable Driver Power Supply Invert Driver External Signal (J1, J2)	1 1	2 +V	3 $\pm$V	4 -V	5 GRD	6 6	7 7	8 8	9 9	10 +5V

As each ROW is used by the programmer, its use should be recorded in the ROW ASSIGNMENT table located on the waveform chart, see figure 3-3, to avoid attempting to use both functions assigned to individual card reader ROWS. Special power applications, necessary external signals, and bussing applications should be considered prior to assigning test signals to card reader ROWS. Once these special requirements (if any) are programmed, test signals can be randomly assigned to the remaining card reader ROWS.

3-5.8 SPECIAL FUNCTION PROGRAMMING. Three special purpose logic functions are provided in the Card Tester to enable the programmer to develop unique test signals required for complex test functions. These special purpose test signals (+SO, +S1, and +S2) are generated from three basic logic circuits utilizing programmable inputs, derived from internally generated test signals, to determine the logic element outputs. The three programmable logic elements include a "D" type flip-flop, an AND gate logic element and a NOR logic element. Using these functional logic elements to develop unique test signals requires special attention from the programmer as the printed circuit card test program is written. Each logic element is individually described below and the technical

characteristics are listed as an aid to the programmer.

3-5.8.1 "D" Type Flip-flop Programming. The "D" type edge triggered flipflop is a high speed logic element used for controlled storage of digital signals applied to the D input and strobed with a positive going clock pulse. The logic symbol, truth table and timing considerations for the programmable flip-flop are shown in figure 3-8.

Timing and operating considerations for the programmable flip-flop are shown in figure 3-8 and delineated below. It should be noted that the flip-flop switching point is approximately 1. 5 volts and the data to be stored in the flip-flop must be present at the "D" input for a period of time (T_{setup}) before the clock pulse crosses this threshold. In addition, the data input ("D" input) must remain at the desired level for a time (T_{hold}) thereafter. Propagation delay (T_{pd}) is measured from the time the clock pulse crosses the threshold to the time the OUTPUT change crosses 1. 5 volts. Additional specific timing and control considerations are listed below:

a. Input data ("D" input) is transferred to the Q output on the positive edge of the clock pulse.

b. Clock triggering occurs at the voltage level of the clock pulse and is not directly related to the duration of the transition time of the pulse.

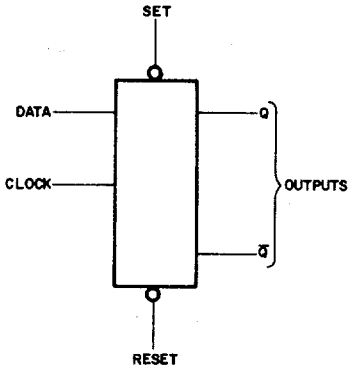
c. Maximum propagation delay (T_{pd}) to switch the Q output to a high level is 35 nanoseconds; maximum T_{pd} to switch Q output to a low logic level is 50 nanoseconds.

d. Low logic levels to SET or RESET inputs take priority over the clock and data inputs.

e. The Q and Q outputs are complementary.

f. Low logic level to SET input forces the Q output to the high level.

g. Low level to the RESET input forces the Q output to the high level.



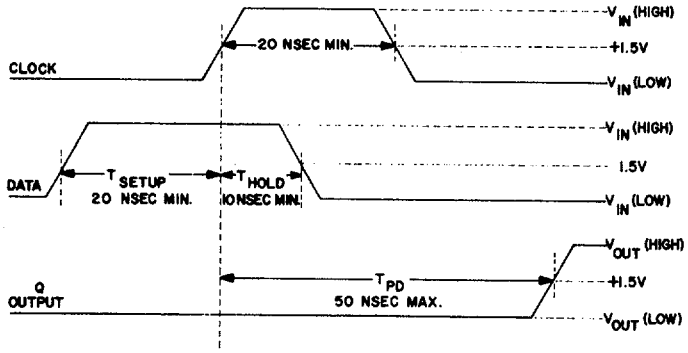
LOGIC SYMBOL

T_N	T_{N+1}	
DATA INPUT	Q OUTPUT	$\overline{Q}$ OUTPUT
0	0	1
1	1	0

TRUTH TABLE

NOTES:

1. 0 = LOW LEVEL
   1 = HIGH LEVEL
2. T_N = BIT TIME PRIOR TO CLOCK
3. T_{N+1} = BIT TIME AFTER CLOCK



TIMING AND PROPAGATION DELAY

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Figure 3-8. D Flip-Flop Logic Symbol, Truth Table, and Propagation Delay

h. The minimum low level pulse width t: either the SET or RESET inputs is 30 nanoseconds.

Several Card Tester test signals are available at the inputs to the programmable flip-flop to allow generation of special output signals to the card under test. These test signals are illustrated in figure 3-9. Each input to the flip-flop has a table which lists the available test signals under program control. For example, the "D" input (+FF STEER) has eight test signals available to be input to the flip-flop under program control. To apply test signal +B5 to the "D" input, simply punch ROW 12, COL 75. In like manner, all other test signals listed in the tables are input to the flip-flop by punching the corresponding ROW and COL into the program test card. Note that both outputs from the flip-flop are available as outputs to the card under test. Either one or the other output can be connected to a given ROW in the card reader matrix but, NOT BOTH. By providing both outputs the programmed test signal (+S1) is available in true and complement form.

3-5.8.2 AND/NOR Logic Element Programming Instructions . Programming instructions for the AND/NOR logic elements require only an understanding of the basic logic element function. The inputs to each element are listed in the tables associated with the logic elements shown in figure 3-10. Truth tables are provided adjacent to each logic element to describe the individual operation. The operational characteristics are not provided, as these parameters are not under program control.

3-5.9 TEST CONNECTOR PIN USAGE. All signals routed into or out of the card under test are routed, via the card reader matrix, through the CARD IN TEST connector (J3) located on the front panel of the Card Tester. This connector is a 56-pin dual edge connector with pin 54 wired to +5V DC and pin 56 wired to logic ground. Each of the remaining 54 pins are connected to the corresponding COL number of the card reader matrix. A CARD IN TEST connector pin is connected to a card reader matrix ROW by simply punching a hole in the desired

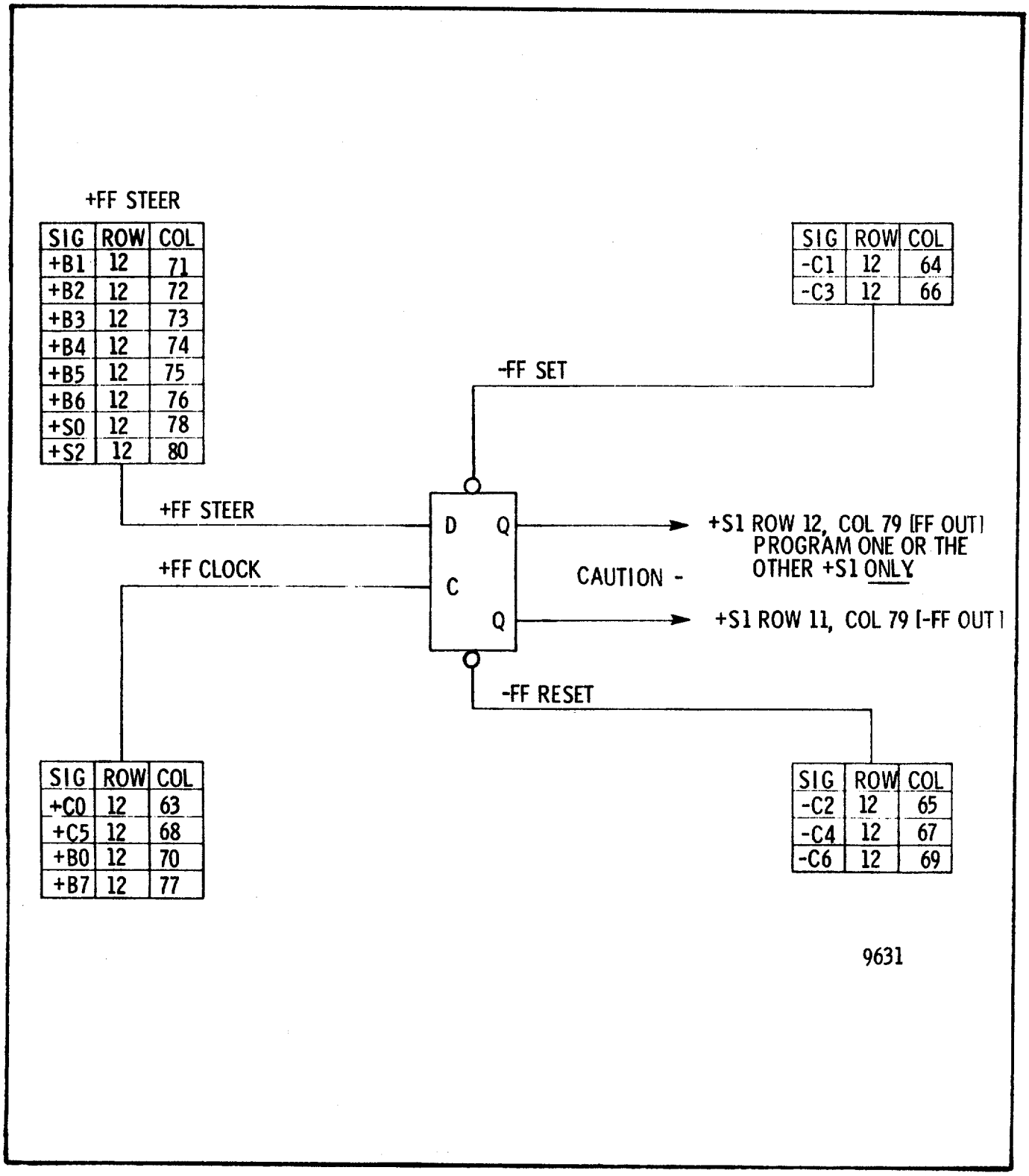


Figure 3-9. "D" Type Flip-Flop Programming Instructions

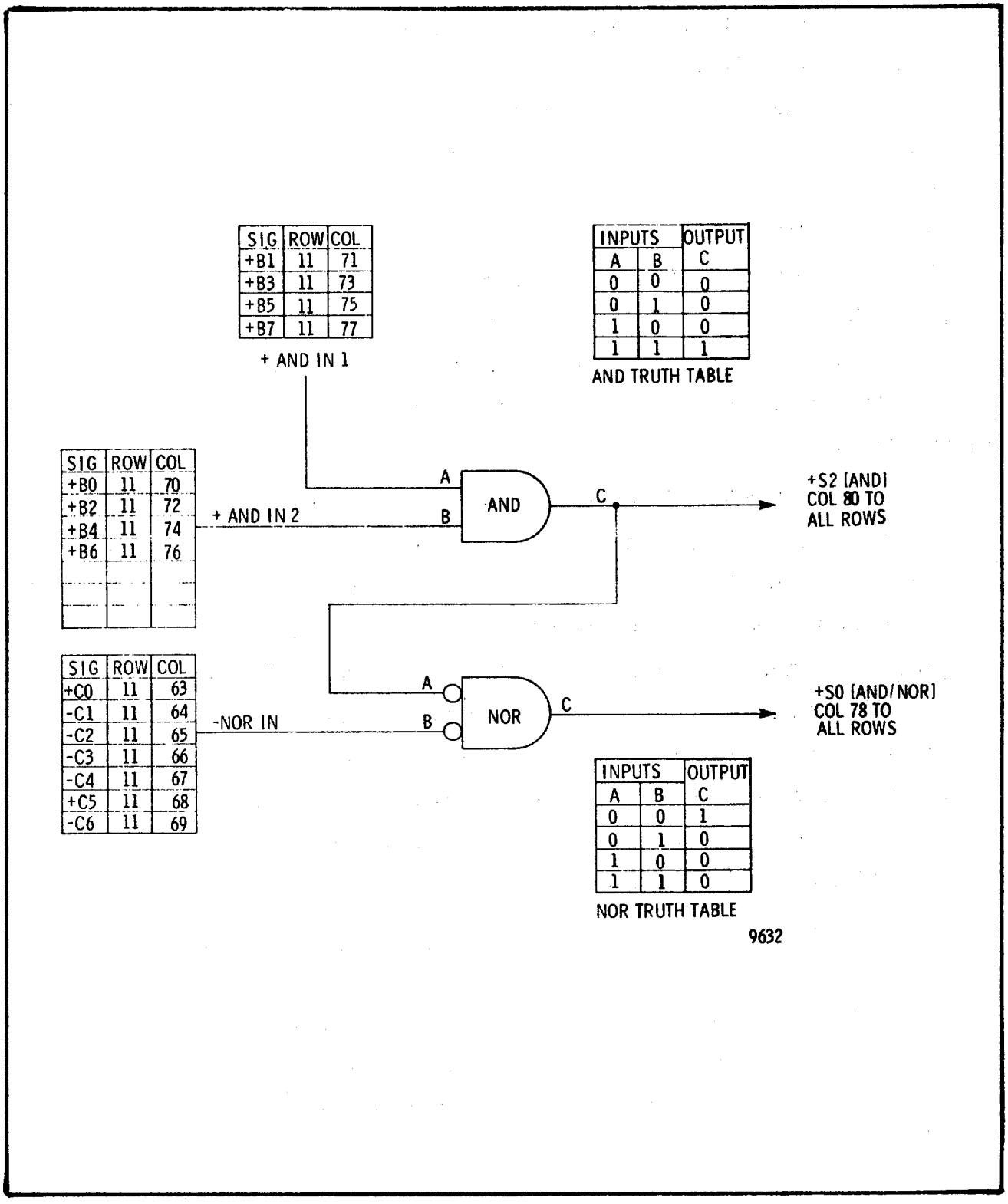


Figure 3-10. AND/NOR Gate Programming Instructions

ROW of the column (COL) corresponding to the pin number. For example, if pins 2, 5, and 7, are to be connected to ROW 3 (ROW 3 being programmed with the desired test signal required on these pins), punch a 3 in columns 2, 5, and 7. If a card adapter is used while programming a particular printed circuit card, refer to the proper adapter cross reference table for pin number correlation between the CARD IN TEST connector and card adapter pin configuration. Card reader matrix group 1 (see figure 3-7) contains the columns associated with the CARD IN TEST pins and schematic diagrams 02-003006 and 02-003007 (see section VII) containing the Card Tester wiring information, signal routing, and matrix cross reference information required for tracing signal flow through the card reader matrix.

3-5.10 TEST SIGNAL INVERSION. Provisions have been made in the Card Tester to invert any of the 18 test signals, under program control, available on columns 63 through 80. Test signals input to programmable drivers number 6, 7, 8, and 9 can be inverted at the input to the driver by programming one leg (input) of an exclusive OR gate. Inputs to the drivers in ROWS 6 through 9 are applied through individual 2-input exclusive OR gates. By programming the second input of the OR GATE to-a high level, the test signal is inverted at the output of the gate and buffered by the programmable line driver. The programming information necessary to invert the test signals applied to programmable line. drivers 6 through 9 is listed below:

	PROGRAM		INVERTS TEST SIGNAL APPLIED TO:
	ROW	COL	
a.	6	54	Programmable driver number 6
b.	7	54	Programmable driver number 7
c.	8	54	Programmable driver number 8
d.	9	54	Programmable driver number 9

3-5.11 TEST RATE PROGRAMMING. Four separate Card Tester clock rates are under program control to allow testing printed circuit card families designed around slow speed, medium speed and high speed logic. When selecting the Card Tester test rate, consideration must be given to the speed of the logic circuits being tested and the propagation delay through the Card Tester and circuit under test. The four Card Tester clock test rates are 1 usec, 2 usec, 32 usec and 16. 39 milliseconds. Propagation delays are most critical with the faster clock rates when signal transitions occur within 1 microsecond of each other. Explanations of the critical propagation delays illustrated in figure 3-11 are given below:

a. BIT PERIOD The time duration between the fastest test signal edges (+BO and +CO test signals). Each of the four programmable bit periods are listed in table 3-6.

b. WINDOW Propagation delay of test signals through the circuit in test. This circuit delay is a function of the speed of the circuits contained on the card in test.

c. SIGNAL DELAY Propagation delay of test signals from signal generator to input pin of the card under test. This delay is a function of the propagation delay of the programmable line drivers and inverter circuits in the Card Tester. Typically the delay is up to 400 nanoseconds for the accumulated programmable line driver and test signal propagation delays.

d. EDGE DETECTOR SET-UP TIME - Time required for Card Tester "Edge Detector" to detect an edge within a given bit period. Typically this time is 100 nanoseconds.

An accumulation of WINDOW time, SIGNAL DELAY time, and EDGE DETECTOR SET-UP time greater than a BIT PERIOD causes erroneous test indications for these measurements. For circuit under test delays of less than 500 nanoseconds, the maximum Card Tester test rate (1 usec bit period) can be programmed without any adverse timing problems. For card under test propagation delays greater than 500 nanoseconds, slower test rates should be

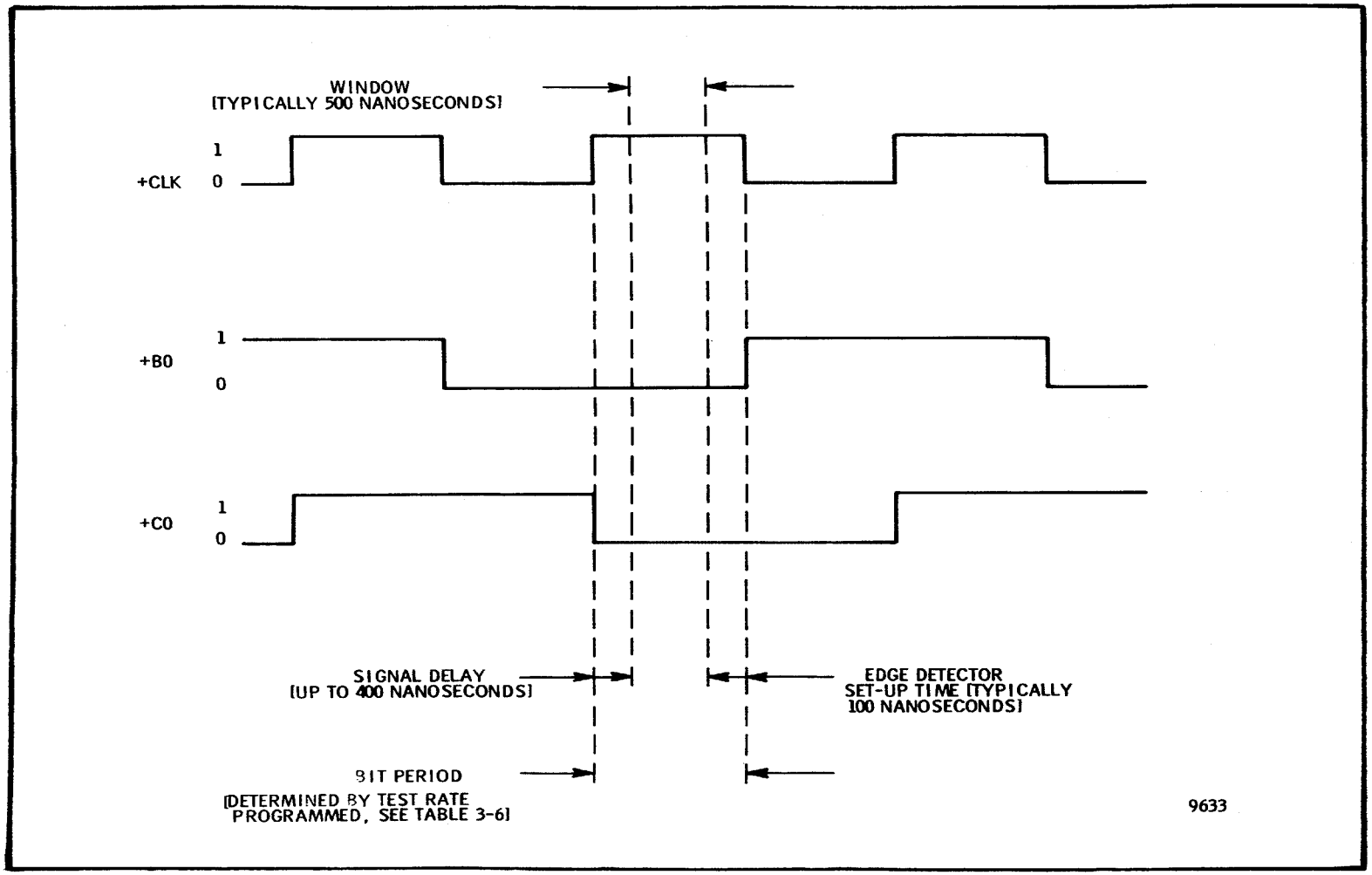


Figure 3-11. Test Rate Propagation Delay Parameters

selected to accommodate the slower circuits being tested. A rule of thumb to follow, Card Tester propagation delays do not exceed 500 nanoseconds for all test rates.

The four programmable test rates available in the Card Tester provide the bit periods listed in table 3-6. Associated programming instructions for each test rate is also contained in the table along with the operating frequency of the fastest test signal, +B0 .

Table 3-6. Programmable Test Rates

PROGRAM		TEST SIGNAL +BO	
ROW	COL	FREQUENCY	BIT PERIOD
2	54	15.25 Hz	16.39 milliseconds
3	54	7.750 KHz	32 microseconds
4	54	125 KHz	2 microseconds
5	54	250 KHz	1 microsecond

3-5.12 LOAD RESISTOR SELECTION AND REFERENCE VOLTAGE PROGRAMMING. Load resistors are provided in the card reader matrix (ROWS 11 and 12) which are connected to any programmable CARD IN TEST connector pin via the program test card. ROW 11, of the card reader matrix, columns 1 through 53 and 55 each contain a 510 ohm resistor connected to the +5 volt power supply output. To connect a card in test output pin to a ROW 1I load resistor the programmer simply punches an 11 in the column corresponding to the desired output pin. ROW 12, of the card reader matrix, columns 1 through 53 and 55 each contain a 3K ohm resistor which, like ROW 11 load resistors, can be connected to any pin on the CARD IN TEST connector. In addition, the programmer must select the reference voltage for the common side of the ROW 12 load resistors. Programming instructions for the ROW 12 load resistor reference voltage follows:

	PROGRAM		CONNECTS COMMON SIDE OF RESISTORS TO:
	ROW	COL	
a.	12	54	+5 Volt power supply output.
b.	12	56	Logic ground bus.
c.	12	57	-V power supply output.
d.	12	58	+V power supply output.
e.	12	59	+V power supply output.

3-5. 13. EXTERNAL INPUT SIGNAL PROGRAMMING INSTRUCTIONS. Signals from an external source are routed into the card under test via the card reader matrix and two connectors on the Card Tester front panel. Connectors J1 and J2 (wired in parallel) are wired to COL 60 of the card reader matrix and are connected to ROW 1 (for distribution to the card under test) by punching a 1 in COL 60.

Note

If ROW 1 is programmed for an external input, DO NOT use ROW 1 for routing test signals to the card under test.

Once the external input connectors are programmed into ROW 1, the external signal can be connected to pins 1 through 53 and 55 of the CARD IN TEST connector using the procedures delineated in paragraph 3-5. 9.

3-5.14 BIT COUNTER OPERATING RATE. Bit Counter operation provides a series of unique points (counts) at which time the card under test output signal edges can occur. The maximum operating rate of the Bit Counter is 1 MHz (programmed with +OSC as the clock strobe) which provides a unique bit count every 1 microsecond. Output signals from the card under test do not exceed 1MHz and therefore will not overrun the Card Tester Bit Counter when it is programmed for maximum counter operation. Under normal conditions the Bit

Counter is programmed with clock +OSC. Each of the four Bit Counter clock rates (TEST RATE equals 1 usec) and associated clock periods are listed in table 3-7. Table 3-8 lists additional clock periods associated with the remaining test rates

Table 3-7. Bit Counter Programming Instructions

PROGRAM			CLOCK PERIOD
ROW	COL	INPUT CLOCK	Test Rate = 1 usec)
9	59	+OSC	1 microsecond
3	59	+CLK	2 microseconds
7	59	+BO	4 microseconds
6	59	+B1	8 microseconds

3-5. 15. SPECIAL CONSIDERATIONS. Programming asyncronous circuits such as oscillators and single shots requires special attention while preparing punched programs. Testing procedures for these type circuits are described in the following paragraphs.

3-5.15.1 Oscillator Programming Requirements. Programming for testing of oscillators requires special considerations in that the oscillator output is asyncronous with the test signals generated in the Card Tester. While testing oscillators, the Bit Counter is disabled (is not programmed) and the Edge Counter is clocked in the normal fashion to cause a GO indication for any setting of the WAVEFORM TEST A switch. The following general steps are required for oscillator program preparation.

a. DO NOT program the Bit Counter (para 3-5. 14).

b. Set the WAVEFORM TEST switch B to (1) for this test.

c. Program the necessary oscillator printed circuit board test parameters (test parameters include power supply voltages, busses, and Card Tester control programming).

d. Set the WAVEFORM TEST switch A to 1. and observe a GO indication for a correct oscillator output. This test does not determine the correct frequency, only that the oscillator output is switching.

3-5.15.2 Single Shot Programming Requirements. Single shot circuit operation presents a peculiar problem to the programmer in that the trailing edge of the output pulse from the single shot is asynchronous with the Card Tester clock circuits. Because of the variable delay from the point the single shot is triggered to the trailing edge of the output pulse, the programmer must select a Bit Counter clock rate which allows for the occurrence of the trailing edge within a specific count of the bit counter. For each trigger into the single shot circuit, two edges are generated. The first edge occurs as the circuit is triggered and the second edge is dependent on the interval of the single shot.

The time duration range between the two output edges of the single shot circuit dictate which Card Tester test rate (para 3-5. 11) and Bit Counter clock rate (see paragraph 3-5. 14) should be programmed. Table 3-8 provides the Bit Counter advance clock time duration (period) for all programmable combinations of Card Tester test rates and Bit Counter clock rates.

Table 3-8. Bit Counter Clock Periods

TEST RATE		BIT COUNTER CLOCK PERIOD			
BIT PERIOD	+BO FREQ	+OSC	+CLK	+BO	+B1
1 usec	250 KHz	1 usec	2 usec	4 usec	8 usec
2 usec	125 KHz	2 usec	4 usec	8 usec	16 usec
32 usec	7.75 KHz	32 usec	64 usec	128 usec	256 usec
16.39 M sec	15.25 Hz	16.39 M sec	32.78 M sec	65.56 M sec	131.12 M sec

A typical single shot output waveform is shown in figure 3-12 to illustrate the thought process necessary to determine the programming parameters required in testing single shot circuits. In this example, figure 3-12, the single shot output pulse occurs from 6. 3 to 7. . 8 usec after the circuit is triggered. The variable tolerance (SS TOL) of the second edge of the output pulse is approximately 1. 5 usec and if adjusted to mid-range, the output pulse would occur near the second negative going edge of test signal +B1. In observing figure 3-12, it

can be seen that of the four possible Bit Counter clock strobes (+OSG, + CLK, +BO and +B1), +BO provides a clock period with sufficient duration to fully cover the single shot tolerance (point (A) to point (B). The Bit Counter must not change at any time during the single shot tolerance. Once a clock is selected which provides a unique count for the duration of the single shot variable tolerance limits, the programmer simply selects the Bit Counter clock period, from table 3-8, which exceeds the single shot tolerance by the closest margin. In this example, the tolerance is approximately 2 microseconds and table 3-8 indicates that a test rate bit period of 1 microsecond used in conjunction with bit counter clock +BO results in a bit counter clock period of 4 microseconds. A four microsecond bit counter clock period allows the bit counter to remain at the count of three long enough for the edge detector to determine that an edge has occurred within the 1. 5 microsecond tolerance. Refer to paragraph 3-5. 11 for test rate programming and paragraph 3-5. 14 for bit counter operating rate programming instructions.

This type of test does not accurately measure the single shot timing but rather checks that the single shot action occurred and that the period is approximately correct.

3-5.16 HOLLERITH SYMBOLS. The card reader has been designed to accept a standard tabulating card which has been manufactured according to EIA Standard RS-292, Media I. The specifications for the manufacture of this type of card used in the card reader were developed by IBM (International Business Machines Corporation). It is imperative that ONLY this type of card be used in the Card Tester card reader. The correct type of tabulating card is easily identified by the rectangular holes in a 12 ROW, 80 COL (column) format, as illustrated in figure 3-13. Included in the figure are the tabulating card nomenclature, numeric information, alphabetic information and special symbol information as punched on a ASR 34 Teletypewriter. The definitions of the terms shown in figure 3-13 are accepted throughout the industry and listed below for the operator/programmer convenience.

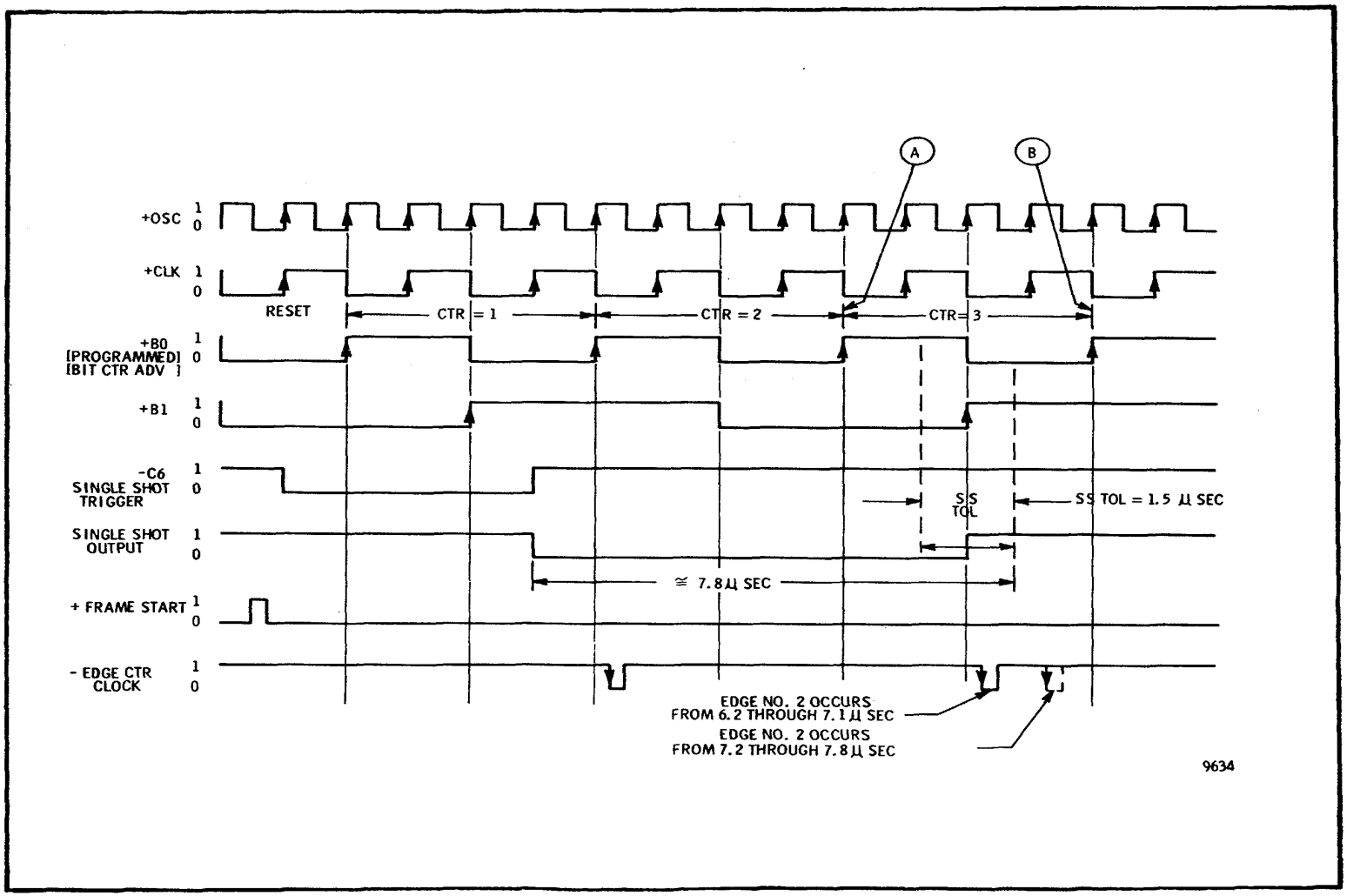


Figure 3-12. Single Shot Programming Example

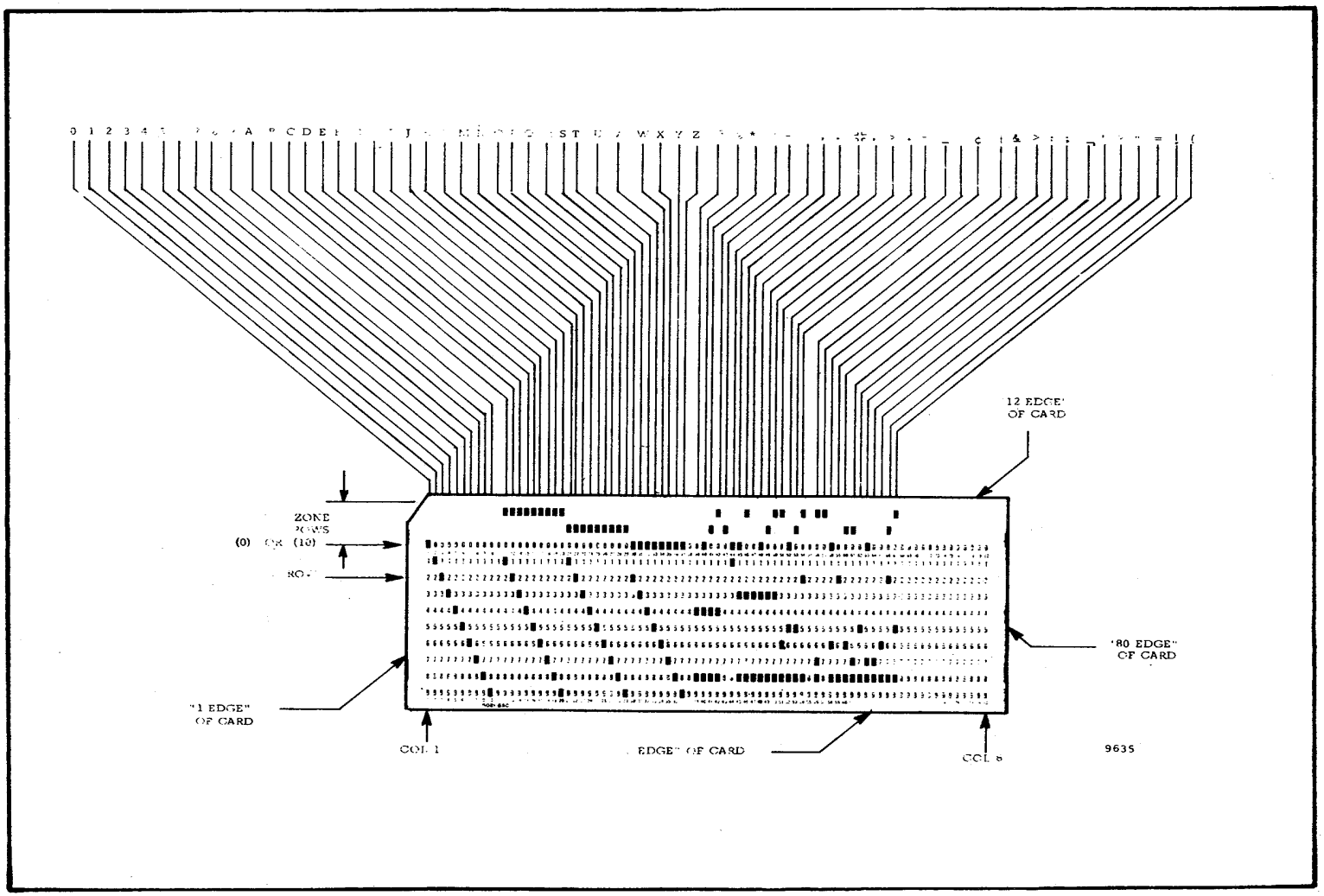


Figure 3-13. Tabulating Card Format/Nomenclature

a. ROW - A horizontal line of digits; all digits in a ROW are the same e. g. , all 8's, all 4's etc.).

b. COL - A vertical line of digits; each COL contains digits 0 through 9 (printed) and 12, 11, at the top (not printed). ROW 0 is sometimes referenced ROW 10; ROW 0 and ROW 10 are one in the same.

c. ZONE ROWS - The three top ROWS, ROWS 12, 11, and 0 (also 10); these ROWS are used for special and alphabetic coding.

d. "9 EDGE" OF CARD - The edge of the tabulating card closest to the "9" ROW; the bottom edge of the card.

e. "12 EDGE" OF CARD - The edge of the tabulating card closest to the "12" ROW; the top edge of the card.

f. "80 EDGE" OF CARD - The edge of the card closest to COL 80; the right hand edge of the card.

g. "1 EDGE" OF CARD - The edge closest to COL 1; the left hand side of the card.

h. CUT CORNER - Cards can be ordered with a cut corner to serve as an aid to determine whether all cards are orientated the same way in a deck.

Note

When ordering tabulating cards for the Card Tester specify the left hand "12" edge to be cut. The card reader will not accept a card other than a left hand "12" cut card.

i. FACE - The printed side of the card.

3-5.17 CARD TESTER PROGRAMMING STEPS. A summary of the programming presented in detail in paragraphs 3-5. 3 through 3-5. 15 is provided below. In addition, group 2 of the card reader matrix is illustrated in detail, figure 3-13, to aid the programmer in preparing a test program for most printed circuit cards. Special applications requiring unique approaches should be attempted only by

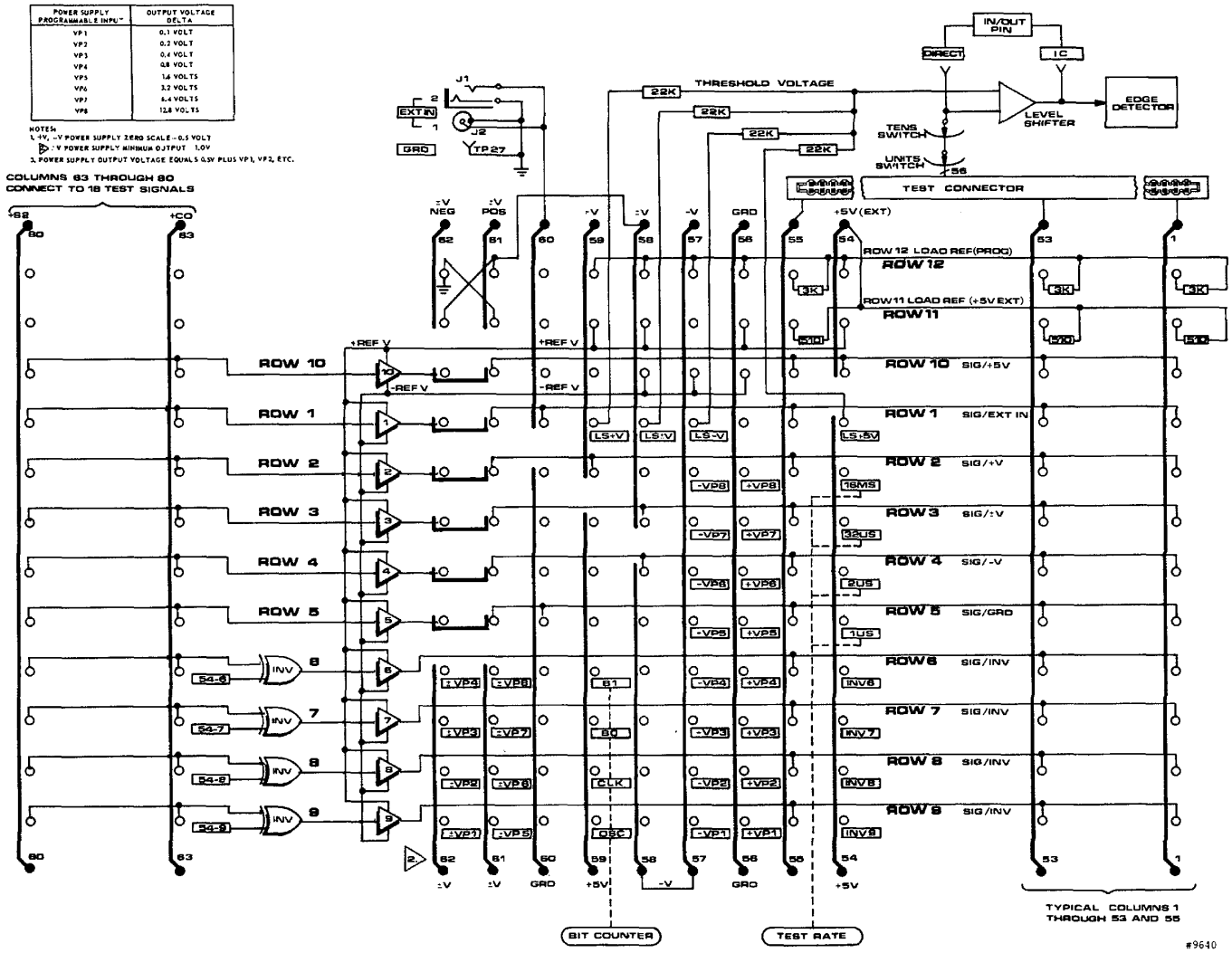


Figure 3-14. Group 2 (Matrix) Exploded View

the experienced programmer. The following steps describe a systematic approach to program preparation and should be adhered to even after the programmer has become proficient in program preparation.

a. Determine the approach required (select test signals for card being tested) to exercise the card under test. Consideration should be given to the following:

1. Special power requirements.
2. Test signals required.
3. Circuit operating speed.
4. External signal(s) necessary.
5. Adapter needed for Card Tester interface.
6. Load resistor values and voltage connections required.

b. List the test parameters, determined in the above step, on the waveform chart as shown below:

TEST PARAMETERS			
V_{CC}		SIG V	
±V		LOAD REF V	
+V		CLK	
−V		BIT CLK	

c. Determine which of the programmable power supply output voltages are to be used and list the power supply selected (any one or all of three) in the appropriate ROW of the ROW ASSIGNMENT table in the waveform chart as shown below:

ROW ASSIGNMENT	
10	
1	
2	
3	
4	
5	
6	
7	
8	
9	

d. If the PC card under test requires a signal from an external source, enter + EXT IN in RO 1 of the chart in c above.

e. If +5 VDC or logic GRD are required on any pins other than pin 54 and pin 56 respectively, in the CARD IN TEST connector, list the required voltage or ground in the chart in c above.

Logic GRD is routed to the PC card under test on ROW 5.

+ 5 VDC is routed to the PC card under test on ROW 1.

f. List the required test signals, which activate the circuits on the printed circuit card, in the ROW ASSIGNMENT in the chart in c above and located in the waveform chart) as needed. Keep in mind that any of the test signals may be inverted (para 3-5.10) and three test signals (+S0, +S1, and +S2) may be generated by the programmer to satisfy special test signal requirements (see paragraph 3-5.8).

g. List all input pins (to the card under test via the CARD IN TEST connector) adjacent to the selected input test signals under INPUT PINS, on the waveform chart e.g., test signal +B0 is to be programmed to pin 37 (input pin of the card under test); the number 37 is written to the left hand side of

test signal +B0. Several pins may require the same test signal and this case all pin numbers must be listed adjacent to the one test signal.

Note

In the following steps, as the program coding is determined, write the necessary coding information in the coding table provided on the waveform chart (also shown in figure 3-14). Once the complete program has been coded, the program is punched into a tabulating card and verified with a working printed circuit card.

h. Program the three programmable power supplies to the voltage(s) required for the card under test, see paragraph 3-5.4.

i. Determine the programmable line driver reference voltage as described in paragraph 3-5.5.

CAUTION

DO NOT exceed 30 volts difference between the + and DVR REF voltages input into the line drivers.

COL	PROGRAMMING
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	
32	
33	
34	
35	
36	
37	
38	
39	
40	

COL	PROGRAMMING	
41		
42		
43		
44		
45		
46		
47		
48		
49		
50		
51		
52		
53		
54		
55		
56		
57		
58		
59		
60		
61		
62		
63		C0
64		C1
65		C2
66		C3
67		C4
68		C5
69		C6
70		B0
71		B1
72		B2
73		B3
74		B4
75		B5
76		B6
77		B7
78		S0
79		S1
80		S2

Figure 3-15. Programming Coding Table

CONNECT		+DVR REF	CONNECT		- DVR REF
COL	ROW	EQUALS	COL	ROW	EQUALS
54	11	+5V	56	10	GRD
56	11	GRD	57	10	--
58	11	+V	58	10	+V
59	11	+V			

Note

When programming +DVR REF and -DVR REF only connect one of the DC voltages in each of ROWS 10 and 11 and ensure that the total difference does not exceed 30 VDC.

j. Determine the level shifter threshold voltage, paragraph 3-5.6, and code the coding table with the necessary coding information.

k. List the required test signals, determined in g above, in the ROW ASSIGNMENT table (waveform chart) and program these test signals to the corresponding ROWS in the card reader matrix, as described in paragraph 3-5.7.

Note

Special function signals are programmed individually as described in paragraph 3-5.8.

l. Route all test signals and power supply outputs previously assigned to card reader ROWS (see ROW ASSIGNMENT table) to the CARD IN TEST connector, refer to paragraph 3-5.9.

m. Program the Card Tester "test rate" . Detailed information required to program the test rate is provided in paragraph 3-5.11.

PROGRAM		TEST SIGNAL +B0	BIT PERIOD
ROW	COL	FREQUENCY	
2	54	15.25 Hz	16.39 milliseconds
3	54	7.750 KHz	32 microseconds
4	54	125 KHz	2 microseconds
5	54	250 KHz	1 microsecond

n. Program the Bit Counter operating rate as listed below. Specific instructions are delineated in paragraph 3-5.14.

PROGRAM		INPUT CLOCK	CLOCK PERIOD
ROW	COL		(Test Rate = 1 usec)
9	59	+ OSC	1 microsecond
8	59	+ CLK	2 microseconds
7	59	+ BO	4 microseconds
6	59	+ B1	8 microseconds

o. Determine the programmable load resistor values required for the circuits under test and program the Card Tester load resistor voltage values, as described in paragraph 3-5.12.

p. Connect the card under test output signal pins (pins in the CARD IN TEST connector) to the load resistors, as described in paragraph 3-5.12.

q. Write the output pin number(s) (grouped for identical output signals) under OUTPUT PINS on the waveform chart. Draw the expected output signal waveform to the right of the SWITCH SETTINGS ('adjacent to the listed pin number) for the corresponding output pin number(s). These output signal waveforms should be drawn with great care to record precise timing relationships with the input signals.

Note

Three waveform charts are available from Dynatronics depicting a full frame, half frame and quarter frame

of input test signals. In many cases the output signals from a given test become repetitive after a quarter or half of a frame. Using a portion of the frame, for these cases, reduces the drawing and drafting time to one-fourth for the quarter frame.

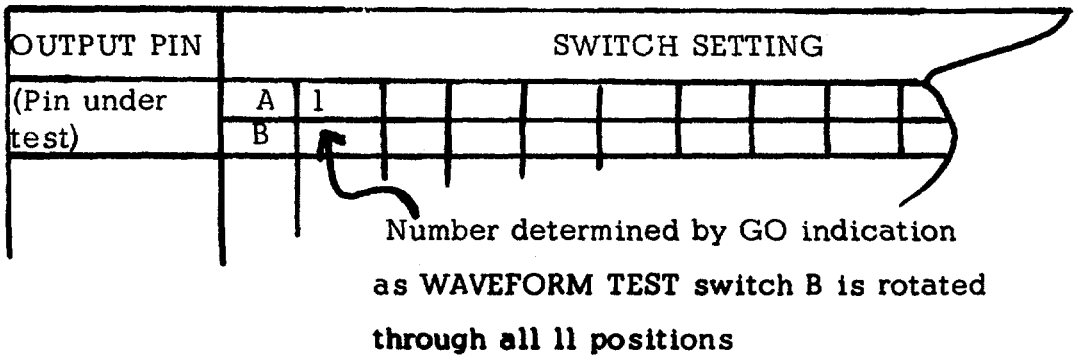
r. Punch the tabulating card with the information recorded in the coding table for the above steps. Hand punches are available for this operation,, see paragraph 1-5.3.

s. Insert the card under test into the card tester, using the necessary adapter and extender if required.

t. Insert the newly punched test program card (tabulating card) into the card reader receiver and rotate the reader handle clockwise until it reaches the mechanical stop.

u. Select the output pin number (Card Tester IN/OUT SELECTOR switches) for the first output signal waveform shown on the waveform chart. Verify the operation of the circuit under test by observing the selected output signal on an oscilloscope (connect oscilloscope to Card Tester IN/OUT PIN, either DIRECT or IC) and comparing it with the input test signals provided on the Card Tester test points.

v. Set the WAVEFORM TEST switch A to position (1) and rotate WAVEFORM TEST switch B until the GO indicator lights. Under the left most SWITCH SETTING, record a (1) for switch A and the position of switch B, as shown below:



w. Increase the position of WAVEFORM TEST switch A by one and rotate switch B through all positions until the GO indicator illuminates. Record the position of switch A and B to the right of the previous entry for this output pin number.

x. Repeat w above until all significant edges of the output signal have been recorded for the selected pin.

y. Repeat u, v, and w above for all output pin numbers listed under OUTPUT PINS (on the waveform chart).

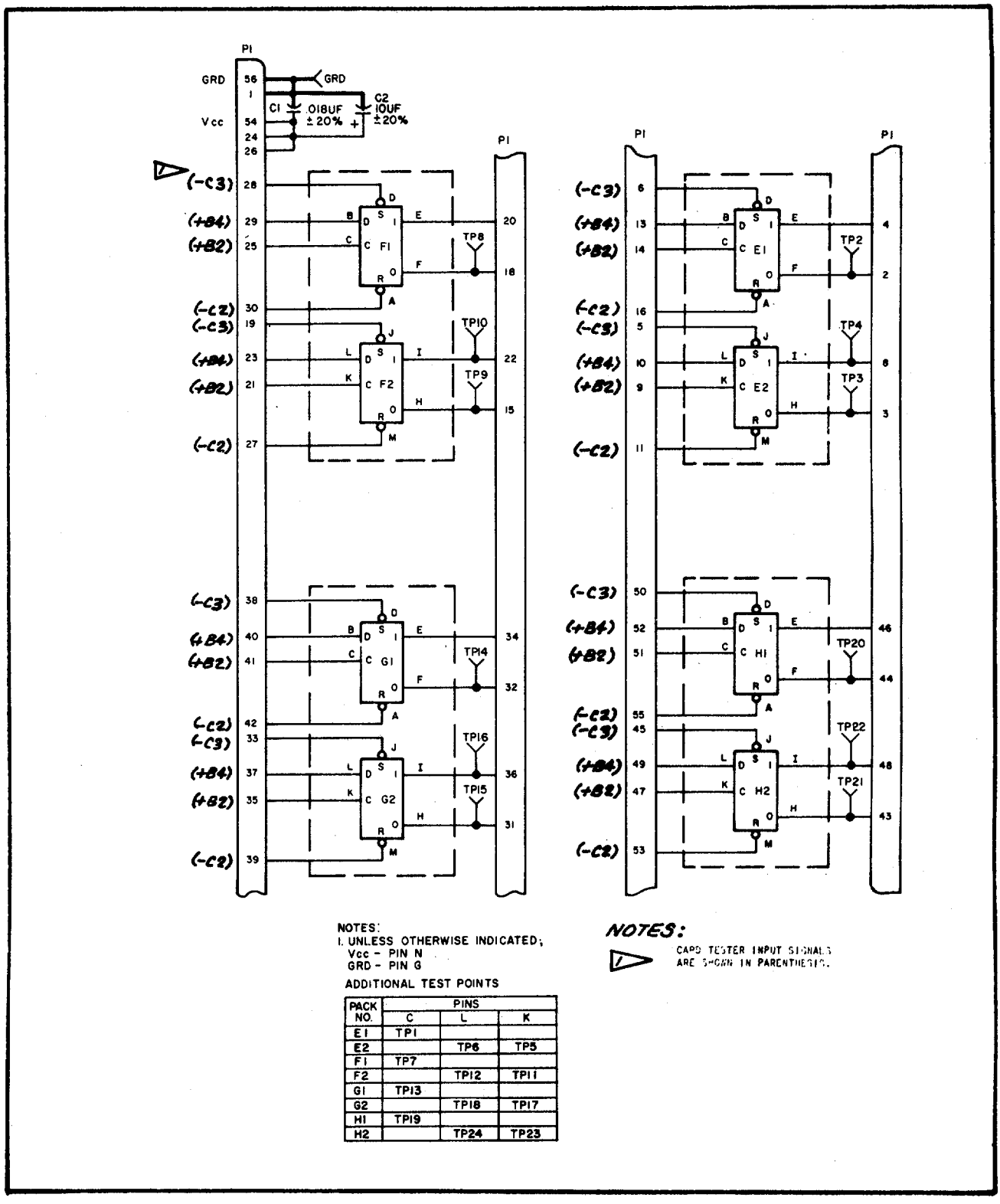
z. Remove the program card from the card reader (rotate the card reader handle CCW until it reaches the mechanical stop) and the printed circuit card from the CARD IN TEST connector.

3-5.18 PROGRAMMING EXAMPLE NUMBER 1. Programming example No. 1 illustrates the steps necessary to prepare, punch, and verify a Card Tester test program for a typical printed circuit board. The printed circuit board chosen for this example is a standard PC card from the Dynatronics card family (type 508-1) which consists of eight dual "D" type flip-flops utilizing TTL series 7400 integrated circuits. The general technical characteristics for this type of integrated circuit are delineated in section VIII. All timing and operational characteristics for the SN7474N integrated circuit are derived from the characteristics given in section VIII.

Each of the eight flip-flops contained on the type 508-1 printed circuit card are tested in an identical manner and the following discussion is with reference to flip-flop F1, shown in figure 3-16. The waveform chart, figure 3-17, contains the example program and all necessary programming information pertinent to its operation. The "D" type flip-flop transfers the information into storage when the clock input switches to a high level (positive going edge). Both the DC set (S) and DC reset (R) inputs override the clock pulse and pull the corresponding output to a high level. For example, a low level into the set input (pin 28) causes the "1" output (pin 20) to switch to a high level. As shown in the example program, pin 28 is connected to test signal -C3 and will cause the true

output (pin 20) to switch to a high level when -C3 swings low. The DC reset input is connected to test signal -C2 causing the true output to change to a low level for the duration of the DC reset pulse (until the DC reset is removed and either another DC set is present or a high level is strobed into the flip-flop via the clock signal). Test signal +B2 has been selected to clock the flip-flop and +B4 is programmed into the "D" input (pin 29). The sequence of events for the flip-flop is shown in the output pin waveform, figure 3-16, for output pin 20. At the beginning of the frame output pin 20 is at a high level (due to last high level of +B4 being loaded into the flip-flop prior to the beginning of the frame) and remains high until +B4 changes to a low level. At the first positive going edge of +B2 after +B4 changes to a low level, output pin 20 swings low. The clock input loads the low level of +B4 into storage. For the next positive edge of +B2, signal +B4 is at a low level and will not change the state of the flip-flop. At -C3 time the flip-flop is DC set, causing the output to toggle to a high level, and at -C2 time the flip-flop is DC reset causing the output to change back to a low level. At the first positive edge of +B2, after the DC reset swings high, a high level is loaded into the flip-flop bringing the output up to a high level again. This sequence repeats itself for the duration of the frame providing a complete functional check for the type "D" flip-flop. As shown in figure 3-17, only the first four edges are checked to provide a complete functional test. The complement output (pin 18) is shown inverted.

3-5.19 PROGRAMMING EXAMPLE NUMBER 2. Programming example number 2 provides a more complex programming situation than example number 1. This example provides the necessary programming information for functionally testing a right/left shift register as contained on a Dynatronics developed printed circuit card. Printed circuit card type 513-1 contains four right/left shift registers which are serially shifted for the first quarter of the frame and then parallel loaded for the second quarter of the frame. The 513-1 card, figure 3-18, is tested by applying the following test signals to the corresponding inputs to each register. Shift register El is used for this example.



PACK NO.	PINS		
	C	L	K
E1	TP1		
E2		TP6	TP5
F1	TP7		
F2		TP12	TP11
G1	TP13		
G2		TP18	TP17
H1	TP19		
H2		TP24	TP23

Figure 3-16. Programming Example No. 1, Dual "D" Type Flip Flop Logic Diagram

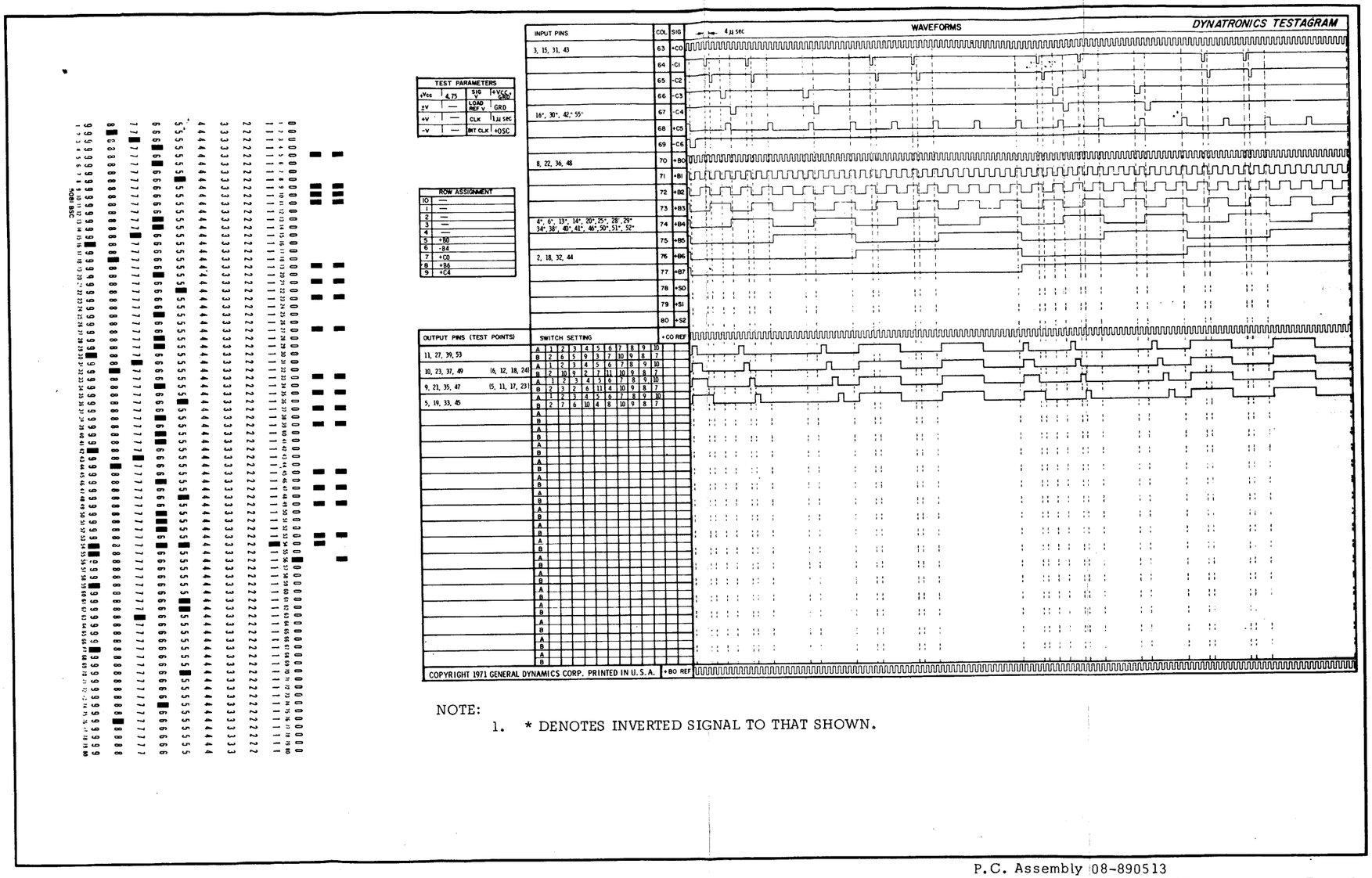
Test Signal	Connects To	Pin No.
-C0	Serial Shift Clock Input	8
+S0	Parallel Load Clock Input	3
+B5	Mode Control Input	2
+C3	Serial Input (Stage 1)	16
+B1 through +B4	Parallel Inputs (All Stages)	13, 14, 6 and 4

At the beginning of the Card Tester frame, test signal +B5 is at a low level and causes a high level to enable the upper AND/OR circuits shown in the schematic diagram, figure 3-18. For the duration of +B5 being at a low level, -C0 is gated into the individual register clock inputs, +C3 is gated into the first stage of the register, and the output from each flip-flop comprising the register is connected to the input of the flip-flop to its right. As the flip-flops are clocked after the start of the frame (+C3 is at a low level) all four register outputs are clocked to a low level and remain low until the +C3 test signal changes to a high level. Test signal +C3 (-C3 inverted by the program) changes to a high level shortly before the first positive edge of +B4 and is loaded into the first stage of the register on the next negative going edge of -C0. Referring to figure 3-19, it is shown that the output from the first stage swings to a high level on the first negative edge of -C0 after +C3 goes high. On the next negative going edge of -C0 the high level in stage 1 is loaded into stage 2 and stage 1 is loaded with a low level (+C3 changed back to a low level). This sequence is repeated until the pulse is shifted through all four stages of the shift register. When +B5 changes to a high level, the mode control gate inhibits the upper AND/OR gates and the lower gates are enabled thus, providing the following configuration for the shift register:

a. The flip-flops are now clocked with +S0 (pin 3).

b. Inputs to each flip-flop are from pins 13, 14, 6 and 4 which are connected to +B1 through +B4 respectively.

As the mode control line changed states (+B5 switches to a high level) each of the four flip-flop outputs are at a low level. As each parallel



NOTE:

1. * DENOTES INVERTED SIGNAL TO THAT SHOWN.

P.C. Assembly 08-890513
P.C. Logic

Figure 3-19. Programming Example No. 2

3-77/3-78

Figure 3-19. Programming Example No. 2

SECTION IV
THEORY OF OPERATION

4-1 INTRODUCTION.

This section describes the operating principles of the Card Tester. The discussions are based on block and logic diagrams. Block diagram is located in this section (fig. 4-1) and the logic drawings referenced are located in section VII. Printed circuit card descriptions, technical characteristics, parts breakdowns and schematic/logic. diagrams are contained in section VIII.

4-2 BLOCK DIAGRAM DESCRIPTION.

The Card Tester performs its testing function by supplying internally generated test signals to the card under test, via an internal card reader, and measuring the elapsed time location of each transition in the output signal, The circuits comprising the Card Tester are functionally illustrated in the detailed block diagram, figure 4-1. A general description, simplified block diagram description, is provided in section I, paragraph 1-3.

Basic timing for the Card Tester begins at the 4 MHz oscillator, located in the upper left hand corner of figure 4-1. As shown, the output from the oscillator is counted down by a Binary Counter providing four independent Card Tester clock rates, selectable under program control. The four divisions of the basic oscillator (1 usec, 2 usec, 32 usec, and 16.4 Milliseconds) are gated into the Test Signal Generator and used to generate the Card Tester test signals. Clock Select Gate control is provided from the card reader matrix and determined by the programmer test capabilities to accommodate various printed circuit card families (low, medium and high speed logic families).

Test signals are generated by the Test Signal Generator providing 15 unique test signals which activate the circuits of the card under test. In addition to the test signals generated in the Test Signal Generator, three programmable test signals (+S0, +S1 and +S2) are generated under program control in the Special Function Generator which is located under the card reader directly below the Test Signal Generator, in the block diagram. Ten of the 18 test signals can be routed to the card under test through the internal card reader ROWS (center portion as shown in figure 4-1). These test signals are connected to individual card reader ROWS via the ten Programmable Drivers, located to the right of the card reader matrix shown in the block diagram. Six of the Programmable Drivers receive test signal inputs directly from the card reader matrix, when programmed; the remaining four Programmable Drivers receive test signal inputs through individual exclusive OR gating elements. These gating elements cause the test signal to be inverted before being applied to the four Programmable Drivers, inverted if programmed on the program card.

Inputs to the Programmable Drivers are standard TTL integrated circuit levels (see technical characteristics in section VIII) and the output signal levels are controlled by the programmer to provide test signals compatible with most printed circuit cards manufactured today. The output test signals from the Programmable Drivers are routed to the card under test under control of the card reader matrix. Each of the ten Programmable Driver outputs is routed through the card reader, to any of 54 pins in the CARD IN TEST connector, through an adapter or extender cable (if required) and then to the inputs circuits of the card under test. These test signals activate the card under test circuits, producing output signals which indicate whether or not the circuits are functioning properly.

Individual output signals, from the printed circuit card under test, are selected by switches UNITS and TENS, level shifted by the Level Shift circuit (providing TTL compatible signals) and applied to the GO/NO'GO Logic circuits for measurement. The GO/NO GO Logic (hereafter Test Circuits) compares each transition of the card under test output signal with the known measurement

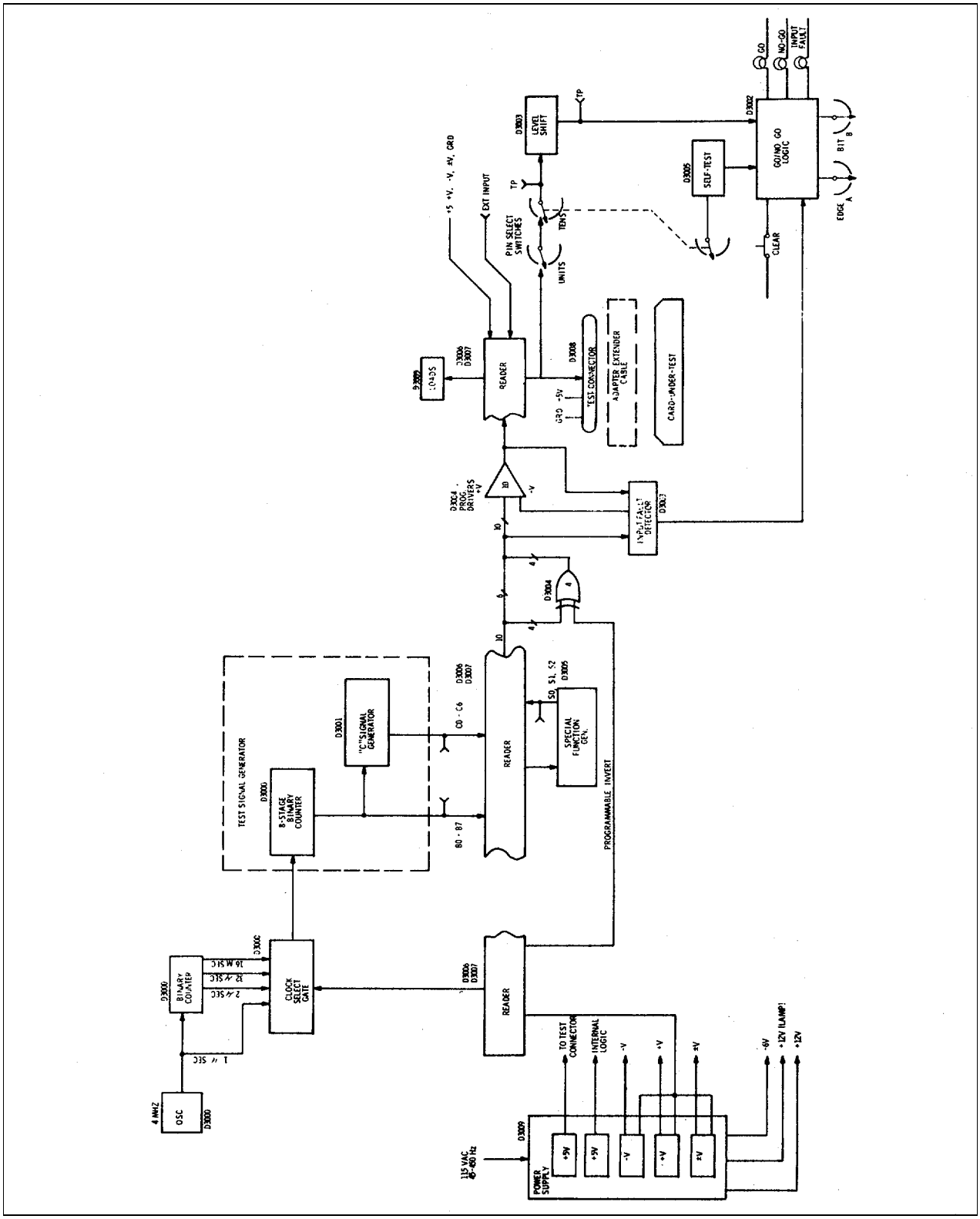


Figure 4-1. Printed circuit Card Tester, Model ICT-102, Block Diagram

selected on the Bit Counter WAVEFORM TEST switch B, shown in the lower right hand corner of figure 4-1. For each transition (selected by WAVEFORM TEST switch A) of the output signal, an individual measurement is automatically made by the Test Circuits and a decision is made indicating the validity of the output signal. As the operator sequences the switches through all measurement points, valid measurements are indicated by the GO indicator as it illuminates. An incorrect output signal is automatically detected by the Test Circuits and indicated by the NO GO indicator illuminating. Additional testing is provided by the Input Fault Detector as it compares the input test signal to each Programmable Driver with the output test signal to determine if any of the output signals have been shorted by the card under test. In the event of a short circuit, the Input Fault Detector automatically isolates the test signal from the input of the Programmable Driver, with the shorted output. Once an input fault is detected (card under test has a shorted input) a red INPUT FAULT indicator is lighted, notifying the operator of the input error.

All power requirements for the Card Tester are provided in the internal power supply which operates from a 115 VAC power source. Three programmable power supplies are included in this power supply which, under control of the programmer, are used to provide special power to the card under test, set the level of the Programmable Driver output signals and set the threshold level of the Level Shifter. These power supplies (+V, -V and +V) are program controlled over a range of 26.1 volts, in 100 milli-volt increments. The outputs from the three programmable power supplies can be routed through the card reader to any one, or combination of, 54 pins in the CARD IN TEST connector on the front panel of the Card Tester. In addition to the three programmable power supply output voltages, +5 volts and logic ground are available under program control to any of the 54 pins in the CARD IN TEST connector.

Individual load resistors are programmable to any of 54 pins in the CARD IN TEST connector providing characteristic load values for the circuits under test. The card reader also controls the power supply output voltage conn

ected to one side of the load resistor thus, providing additional versatility to accommodate numerous card families.

4-3 CLOCK SIGNAL GENERATION.

Internal timing of the Card Tester is controlled from a bisic 4 MHz oscillator, located in the upper left hand corner of drawing D3000, see section VII. The four MHz output of the oscillator (labeled +FREQ) is applied to PC card 1A-14 where it is divided down by three divide-by-16 counters and one divide-by-8 counter to 122 Hz. Four taps are brought out of the counters providing the four basic Card Tester operating rates. These four operating rates are 2 MHz, 1MHz, 62o5 kHz and 122 Hz and are routed to the test signal generator through the Test Rate Select Rate gates.

4-4 CLOCK SELECTION.

Selection of one of four Card Tester operating rates is provided by the Test Rate Selection Gates shown in the lower left hand corner of D3000. Two inputs to each of the four gating elements consist of one of the basic Card Tester operating frequencies (from the clock signal generator counters) and a gate control (enable) line from the card reader matrix, see D3006. Clock control lines (+CLK 1 through +CLK4) from the card reader matrix are tied to logic ground through a 470 ohm resistor to inhibit all gates until the programmer selects a particular gate using the program card. When selected, a particular gate clock control input is connected to +5 Volts through the card reader enabling the corresponding operating frequency input from the oscillator circuits. The output from the Test Rate Select Gates, +2 OSC, is routed to the following: a. "B" Clock Generator to generate test signals.

b. "C"' Clock Generator to generate a frame start signal.

c. Edge Compare Circuit to provide card under test output signal edge compare timing pulses.

d. Self Test Circuits to provide self test clock pulses for TEST 2.

Refer to paragraph 3-5.11 for programming information regarding the use of the available Card Tester test rates.

4-5. TEST SIGNAL GENERATION.

Internal Card Tester test signals are generated by three separate signal generators. Detailed descriptions of the "B" Clock Generator, "C" Clock Generator and Special Function Clock Generator are provided below.

4-5.1 "B" SIGNAL GENERATOR. Eight test signals (BO through B7) are generated in the "B" Clock test signal generator, shown in the lower right of D3000. These test signals (+BO through +B7) are the outputs of cascaded binary counters G1 and HI and are derived from the basic Card Tester operating frequency, as selected by the Test Rate Select Gates. Refer to the waveform chart INPUT WAVEFORMS, figure 3-3, which illustrates the timing relationships between the "B" test signals. In drawing D3000, it is seen that the output from the Test Rate Select Gates, 1A-Al, is applied to flip-flop 1A-Jl. The output from flip-flop IA-J1, +OSC, is applied to the clock input of "D" type flip-flop L1, to again divide the operating frequency in half. For example, if 2 MHz is gated through the Test Rate Select Gates, +2 OSC equals 2 MHz, +OSC equals 1 MHz and the output of flip-flop 1A-Li (+CLOCK) equals 500 kHz. Flip-flop output L1, pin E, is connected t, divide-y-16 counter G1, pin P, to provide "B" test signals +BO through +B3. Test signal +BO, for the above example, is output at 250 kHz and each stage from the counter divides this basic frequency by 2. Test signal +B3, output from divide-by-16 counter G1, is tied to the clock input to divide-by-16 counter HI providing test signal output +B4 through +B7. The test signal generated in the "B" clock signal generator is routed to the card reader matrix, for connection to the Programmable Driver inputs; to the front panel test points, for monitoring card tester operation and comparing card in test output signal timing; and to the "C " Clock signal generator, for generation of timing and control test signals.

4-5.2 "C" SIGNAL GENERATOR. The "C" Clock signal generator provides seven unique test signals used for timing and control pulses which are not edge

coincident with the eight "B" Clock test signals. By utilizing the right combination of "B" and "C" clock signals the programmer can avoid generating overlapping control functions which cause spurious edges by the card under test gating circuits.

By using a "C" clock to trigger a flip-flop containing a "B" test signal on its input, the flip-flop changes at either a high or low level and not at a point where the input is changing (if a "B" clock were used to trigger the flip-flop). An initial phase shift of 900° from the "B" signal phase is provided by flip-flop 1A-L2 (see D3000) for the "C" test signals. Flip-flop L2 is triggered by +CLK (as is divide by-16 counter G1) on the positive going edge but, GI (the first stage of which generates +BO) is clocked by a negative going edge of +CLK and the output (+BO) is applied to the "D" input of flip-flop L2. In this manner the output from flip-flop L2 lags the +BO test signal by 90'. Figure 4-2 illustrates the timing relationship between test signals +BO and +CO.

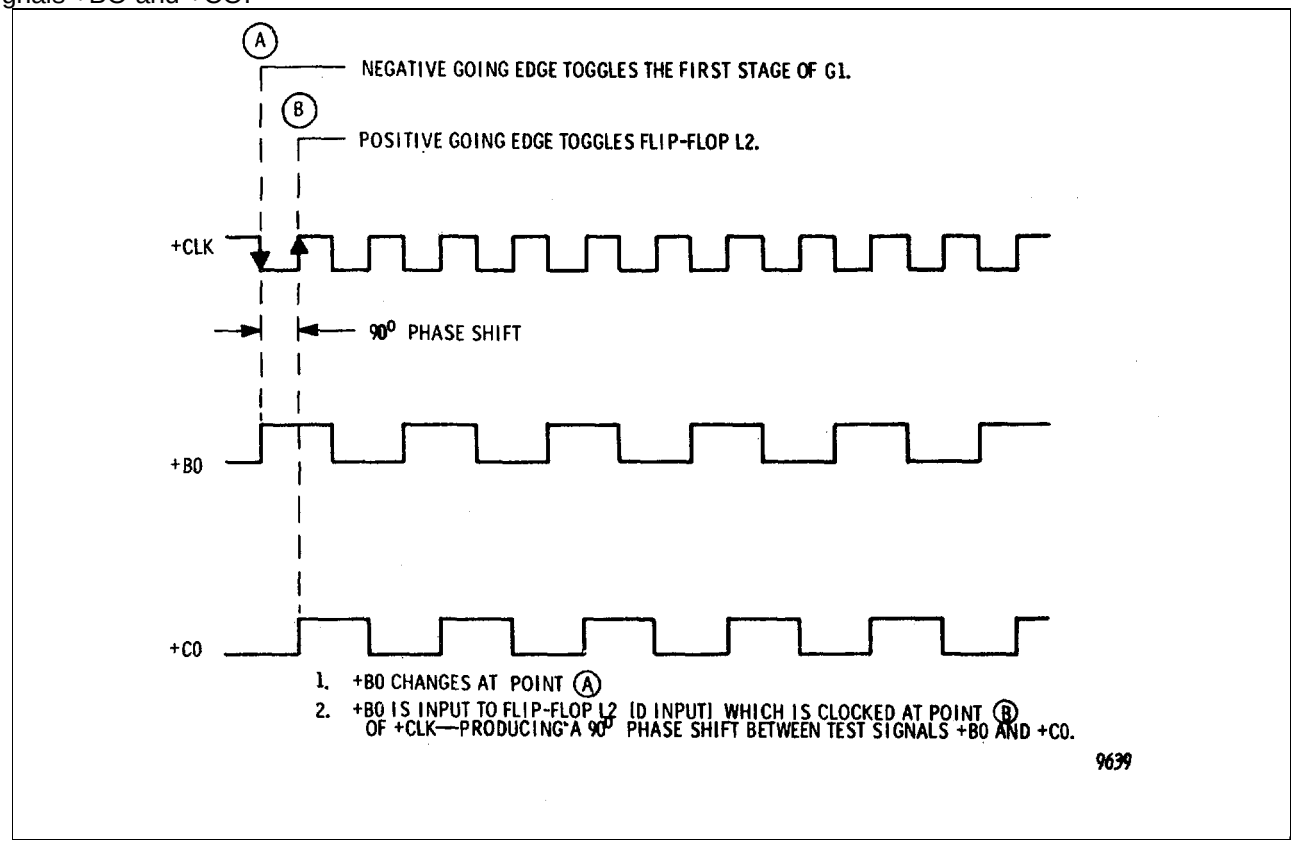


Figure 4-2. Test Signal Phase Relationship

The "C" Clock Generator is located on drawing D3001, contained in section VII. Referring to D3001, note that test signals +BO through +B3 are input to a binary to unitary decoder (K1 in the upper left hand corner of the logic diagram) with unitary outputs 0, 6, 8, 12 and 14 being used to generate "C" phase signals. The unitary output signals represent the binary counts of the BO through B3 stages of the "B" Clock Generator. Each of the unitary outputs from the decoder is used to develop a unique "C" phase test signal when additional decoding is provided by the gating elements to the right of the decoder. The relationship between the unitary outputs and "C " test signals is listed below:

a. Unitary output 6 corresponds to test signal -C1.

b. Unitary output 8 corresponds to test signal -C2.

c. Unitary output 12 corresponds to test signal -C3.

d. Unitary output 14 corresponds to test signal +C5.

e. Unitary output 0 corresponds to test signal -C4 and -C6.

Referring to figure 3-3, note that test signals -C1 and -C2 have a pulse duration equal to one-half of a +CO cycle and the remainder of the "C" test signals have a pulse width equal to a complete +CO cycle. The pulse duration is determined by the clock applied to the six flip-flops on the right of D3001. 'Flip-flops C1 and C2 (which provide test signals -C1 and -C2) are clocked by OSC and flip-flops B1 through B4 (which provide test signals -C3 through -C6) are clocked by +CO. Internal clock signal -OSC operates at twice the frequency as +CO thereby providing output test signals at one-half the pulse width. Test Signals +CO0 through -C6 are routed to the card reader matrix (for connecting to the Programmable Driver inputs) and to the front panel test points (for Card Tester monitoring and card under test output signal comparisons.

All Card Tester timing operations are based on the beginning of the frame as decoded by the Frame Start Decoder sh6wn at the bottom of D3001. NAND gate F3 is trued when the following signals are at a low level +B4, +B5, +B6, +B7

and the "0" output from binary-to-unitary decoder K1. NAND gate JI is trued (output at a low logic level) when -CLK, -OSC and +OSC delay are at a high logic level. When both NAND gates (T1 and P3) are trued (at low logic levels) gate E3 provides a positive output (high level) which is the decoded frame start pulse, +FR START. Minus FR START resets the GO/NO-GO Test logic at the beginning of the frame and is used by the Self Test logic circuits. Plus FR START is wired to the SYNC test point on the front panel to provide the operator/programmer with an external synchronization pulse to trigger an oscilloscope. See figure 4-7 for the timing relationship between the test signals and the frame start pulse generated by the Frame Start Decoder.

4-5.3 SPECIAL FUNCTION SIGNAL GENERATOR. Three special purpose test signals are available in the Card Tester; generated by the Special Function Generator, shown in drawing D3005. These three logic elements, upper right hand corner of the drawing, are under program control through the card reader matrix to generate test signals +SO, +S1 and +S2. Flip-flop 3A-B2 e.g., is clocked by signal +FF CLK which is input from D3006. Drawing 3006 contains one-half of the card reader matrix (columns 41 through 80 and the clock input is tied to ROW 12 COL 77 (12C77) of the card reader matrix. Referring to D3006, the third signal from the top left hand corner of the drawing is +FF CLK which connects directly to ROW 12 columns 63, 68, 70 and 77. These four columns contain -CO, +C5, +BO and +B7 in the order of the columns given above. The programmer can connect any one of these four columns (through the punched program card) to ROW 12 which causes the corresponding test signal to be connected to the flip-flop (3A-B2) clock input. In this manner, the remaining inputs to the flip-flop are controlled by the programmer to generate a unique test signal for special programming requirements. Figures 4-3 and 4-4 provide a simplified illustration of the test signals and card reader interconnection between the test signals and Special Function Generator logic elements. It should be noted that both outputs from the flip-flop, figure 4-3, are available to the programmer to provide both the true and complement form of the programmed

test signal. Only one output should be programmed at a time. Section III, paragraph 3-5.8.1 provides the detailed technical characteristics for the "D" type flip-flop .

4-6 CARD READER MATRIX CONFIGURATION.

The card reader matrix is a 12 ROW by 80 COL contact arrangement and is used to connect Card Tester test signals to the card under test and route the necessary internal control signals throughout the Card Tester. Contact springs make connections between the ROWS and COLS each time a hole is provided in the proper location on the tabulating card. Basically the card reader matrix serves as a 960 contact switch whereby all connections, as selected by the hole pattern in the tabulating card, are completed simultaneously.

Card reader matrix wiring diagrams are illustrated on drawings D3006 and D3007, see section VII. D3006 provides the wiring and signal cross reference numbers for columns 41 through 80 (ROWS 1 through 12) while D3007 shows columns 1 through 40 of the matrix. Figure 4-5 provides a simplified layout of the card reader matrix as viewed from the tabulating card structure. In general the 12 ROW by 80 ('OL matrix is divided into three main groups to control signal routing, power supply programming and internal Card Tester control functions. Group 1 consists of 54 pins connected to the CARD IN TEST connector (J3) on the Card Tester front panel. Any of the 18 internally generated test signals and power supply outputs can be connected to any or all of the 54 pins on the test connector. Group 2 consists of an area dedicated to program control parameters for the Card Tester and group 3 provides the test signal routing and distribution area. ROWS 1 through 10 in the test connector routing area (group 1) are used to route power supply output voltages and test signals to the card under test (via the CARD IN TEST connector) ROWS 1 through 10 are described below:

a. ROW 1 Driven by any test signal connected to line driver number one or used to route an external input (connected via j1 or J2 on the front panel) to the card under test.

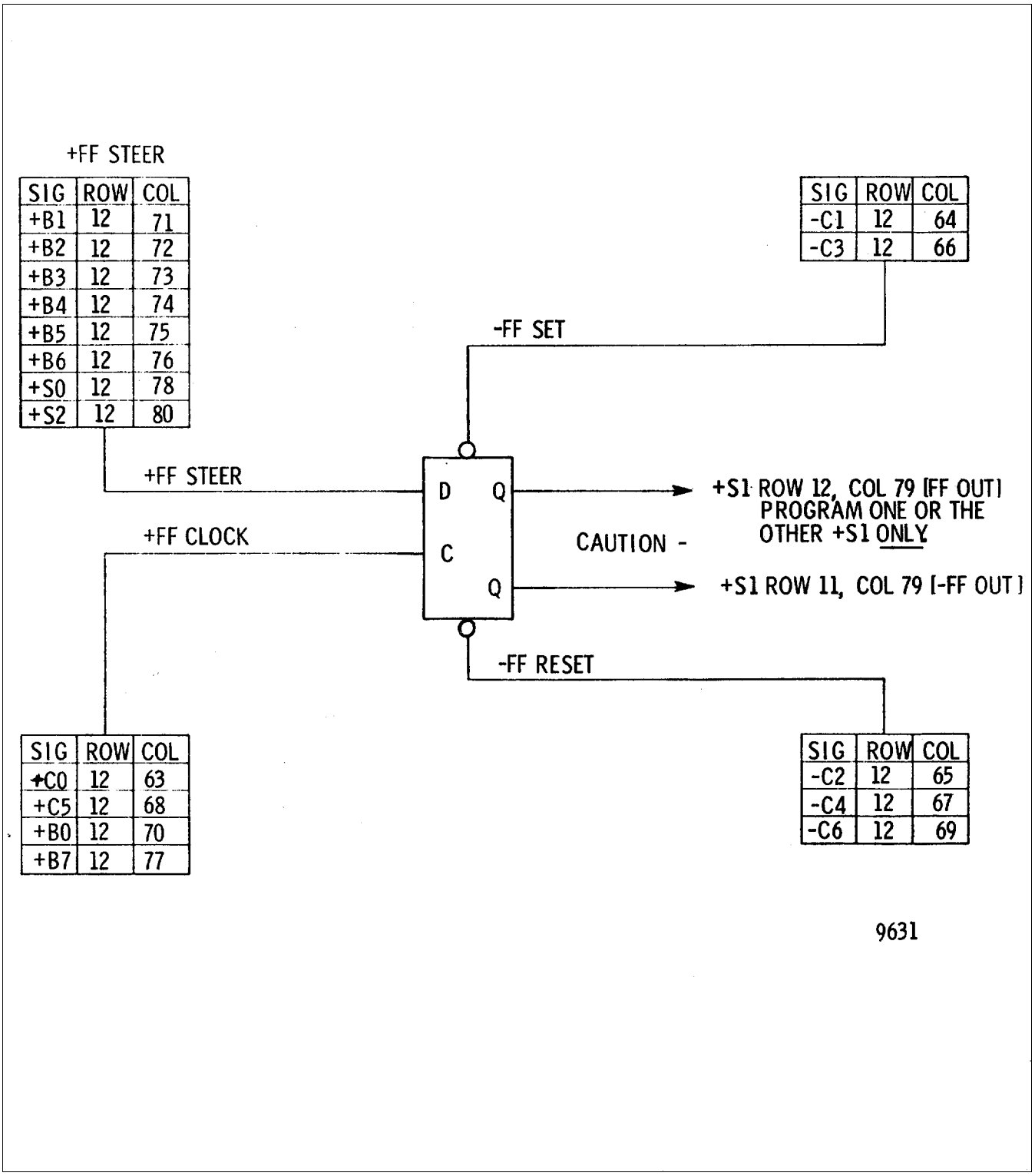


Figure 4-3. "D" Type Flip-Flop Programming Instructions

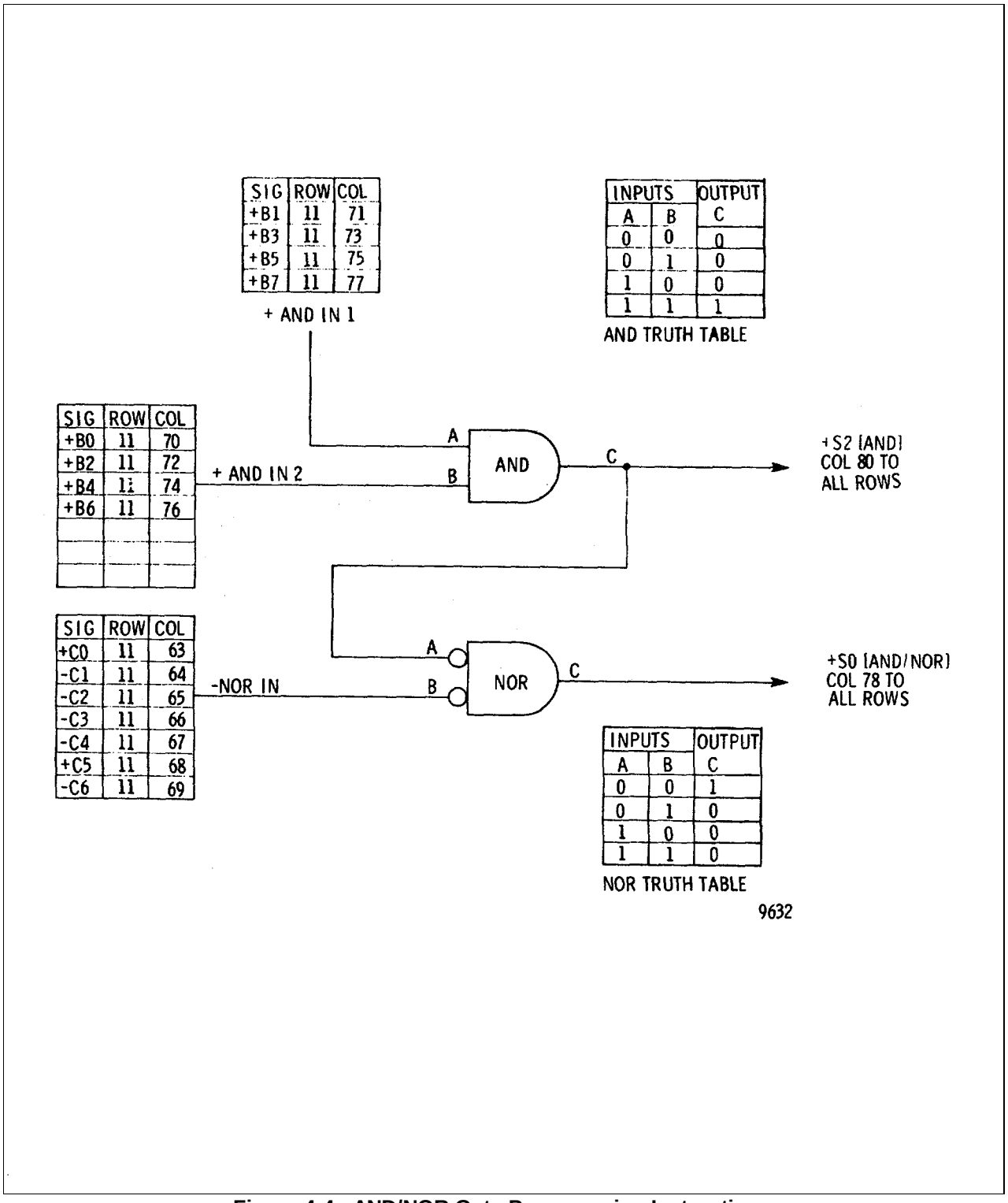


Figure 4-4. AND/NOR Gate Programming Instructions

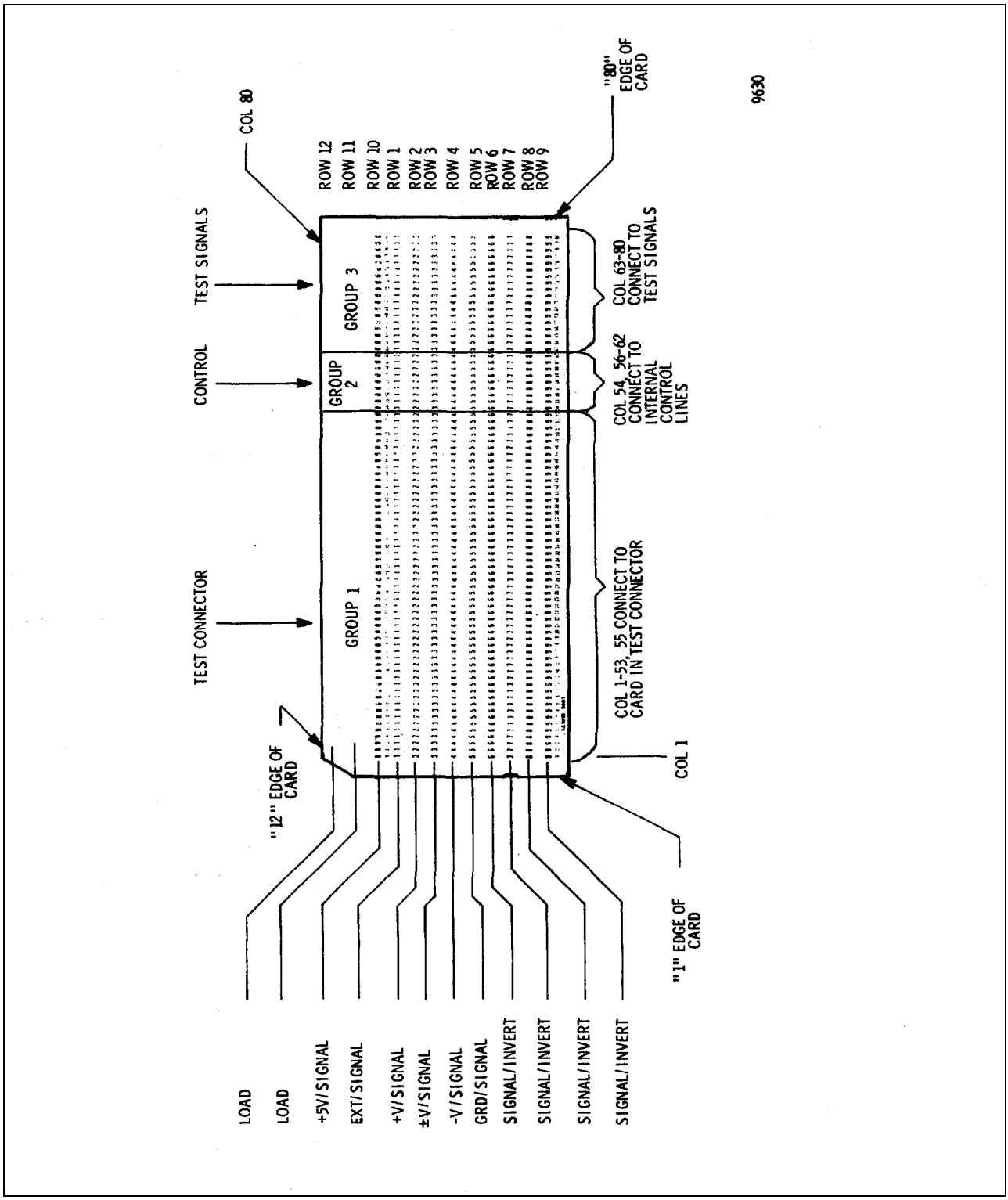


Figure 4-5. Card Reader 12 X 80 Matrix Layout

b. ROW 2 Used either to route any programmed test signal from line driver number two or the output from the +V power supply to any pin on the CARD IN TEST connector on the front panel.

c. ROW 3 Routes either the output from the +V power supply or the output from line driver number three to any pin on the CARD IN TEST connector on the front panel.

d. ROW 4 -Routes either the output voltage from the -V power supply or the output from line driver number four to any pin in the CARD I N TEST connector on the front panel.

e. ROW 5 Routes either power ground or the output from line driver number 5 to any pin on the CARD IN TEST connector on the front panel.

f. ROW 6 Routes either the true or complement form of any test signal applied to line driver number six to any pin on the CARD IN TEST connector on the front panel. The test signal may be inverted.

g. ROW 7 Same as ROW 6 above except uses line driver number seven.

h. ROW 8 Same as ROW 6 above except uses line driver number eight.

i. ROW 9 Same as ROW 6 above except uses line driver number nine.

j. ROW 10 Provides a connecting path from either line driver number 10 (which buffers all test signals from COL 63-80) or the +5 VDC EXT power supply output to any pin on the CARD IN TEST connector on the front panel.

Inputs to the line drivers described above are determined by the programmer and instructions for their use are described in paragraph 3-5.7.

4-6.1 GROUP 1 STRUCTURE. Group 1 of the matrix provides connections between ROWS 1 through 10 and any of 54 pins on the CARD IN TEST connector, as shown in drawing 3007. For example, a test signal applied to ROW 3 is connected to pin 13 of the CARD IN TEST connector by locating a punched hole in ROW 3, COL 13. Punching a 3 in column 13 of the tabulating card makes the above connection; additional pins are connected to the same ROW by punching a 3 in the corresponding column (s). Any of the ROWS may be used for connecting several CARD IN TEST connector pins together by simply punching the necessary

columns (corresponding to the desired pin numbers) with the number of the selected ROW.

4-6.2 GROUP 2 STRUCTURE. Group 2 of the card reader matrix provides programmer control for the internal Card Tester control parameters, as illustrated in figure 4-6. This simplified diagram of group 2 of the matrix shows the internal circuitry associated with the matrix; used to control the Card Tester operation. Due to the complexity of the matrix and associated circuitry, each area is briefly described below to provide a general understanding of the control functions performed by the matrix. Detailed operation of the circuits evolved are provided in section III (programming instructions) and under separate paragraphs in this section. The following discussion is based on the information illustrated in figure 4-6.

Card Tester test rates (four individual programmable rates) are controlled from COL 54, ROWS 2, 3, 4 and 5 as shown in the center right side of the drawing. Gates 1 through 4 are inhibited (by the pull down resistors) until enabled by a punched hole in COL 54, ROW 2, 3, 4 or 5 which applies +5 volts to one of the lower input legs, gating the associated test rate clock to the signal generators (see paragraph 4-4).

Level Shifter operation (upper right hand corner of figure 4-6) is controlled by the voltage value on the input resistors (see paragraph 3-5.6). One or all of four power supply output voltages are applied to the Level Shifter by connecting ROW 1 to column (s) 54, 57, 58 and/or 59. Columns 57, 58 and 59 are connected to the programmable power supply output voltages which are determined by the card under test voltage requirements for individual printed circuit cards. The Level Shifter level shifts the output signals from the card under test to TTL compatible signals which are routed to the internal Card Tester Edge Detector circuits. The threshold point for the Level Shifter is normally calculated to equal one-half the card under test output signal peak-to-peak voltage level.

External test signals, to be input to the card under test via the card

reader matrix, are connected to J1 or J2 (upper left hand corner of figure 4-6). These connectors, JI and J2, are wired in parallel to column 60 of the matrix which can be connected to ROW 1 (and input to any of 54 pins in the CARD IN TEST connector) by punching COL 60, ROW 1. Once programmed, the external test signal is connected to pins 1 through 53 and/or 55 of the test connector as described for the matrix group 1 signals.

Bit Counter clock rates are controlled in group 2, as shown in the lower right hand corner of figure 4-6. Internal Card Tester clock signals are gated into the Bit Counter clock input under control of the programmed test card. Column 59, ROWS 6, 7, 8 and 9 connect the gate enable input legs to +5 volts each time a hole is punched in the corresponding COL/ROW location. When not programmed, each gate is inhibited by the pull down resistors which are wired to logic ground. Programming instructions for the Bit Counter clock rates are delineated in paragraph 3-5.14 and the card reader matrix is illustrated in drawing D3006, section VII.

Programmable power supplies (+V, -V, +V) are controlled from the card reader matrix, group 2. Eight inputs are provided for each of the three power supplies to control the power supply outputs over the range of 1 through 26.1 volts for the +V supply and 0.5 through 26.1 volts for the +V and -V supplies. Each of the power supplies is located along the lower portion of figure 4-6 with their corresponding programmable inputs located above the power supply in the card reader matrix. Programming instructions for the power supplies are provided in paragraph 3-5.4 and the power supply wiring information is presented in drawing D3009. A detailed discussion of individual power supply operating principles is provided in paragraph 4-3 and drawing D3010 contains the internal power supply circuits. Columns 61 and 62 (ROWS 11 and 12) control the polarity of the output voltage from the +V power supply. Refer to the programming instructions for detailed users instructions regarding the polarity controls.

Ten Programmable Drivers are located along the left hand portion of figure 4-6. These drivers provide the necessary drive capabilities to output 100 milliamperes of current over a range of +24 volts unipolar or 30 volts peak

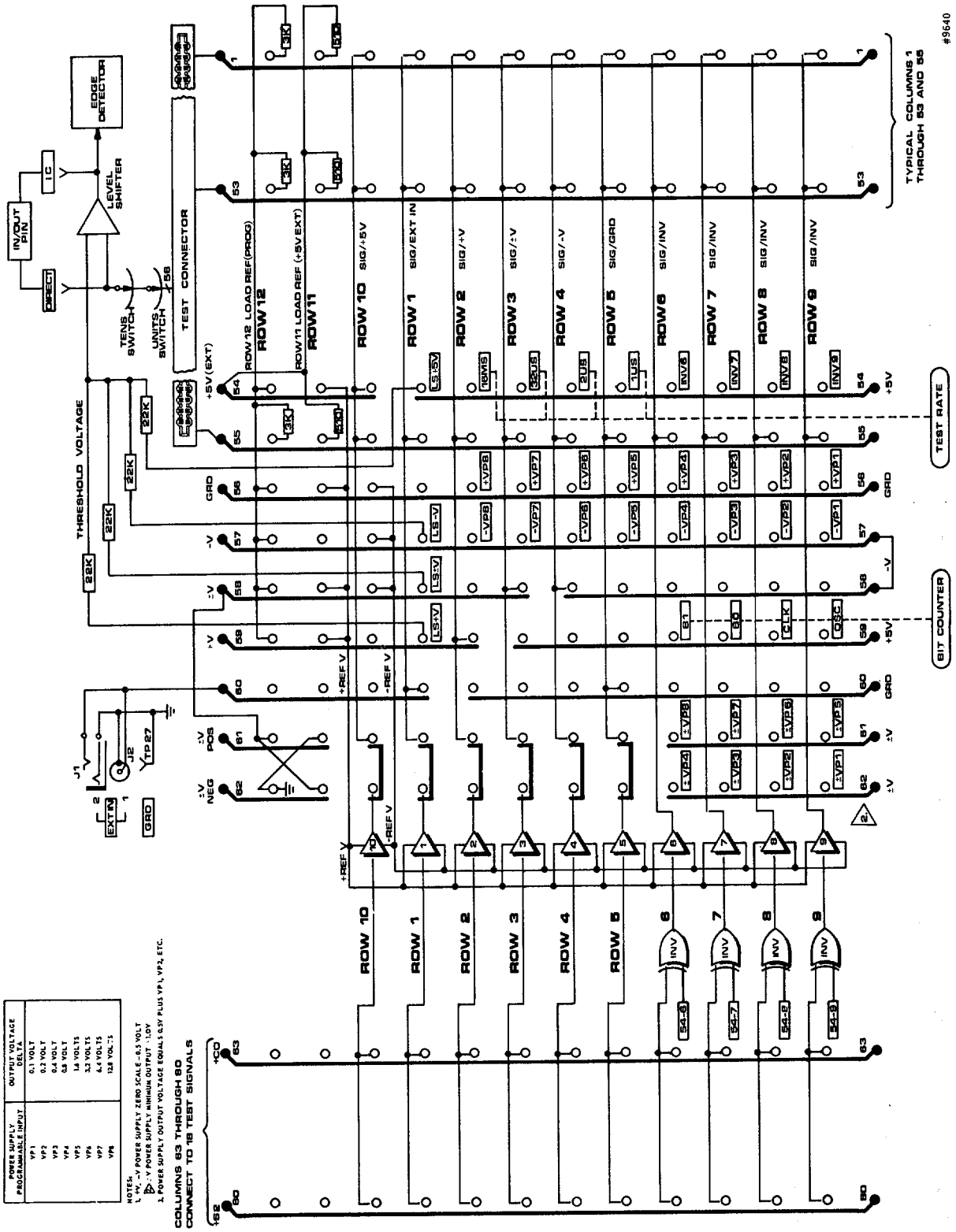


Figure 4-6. Group 2 (Matrix) Exploded View

to-peak, symmetrical or non-symmetrical. All 18 test signals are available at the inputs to each Programmable Driver (input control is located in group 3 of the matrix) as illustrated by COL 63. Column 63 extends down through all 12 ROWS of the matrix making test signal +C0 available at the inputs to each of the ten drivers. To input +CO into Programmable Driver number 4 e.g., the programmer merely punches a 4 in column 63 (punch ROW 4, COL 63). The remaining 17 test signals extend from COL 64 through COL 80 and are input to the Programmable Drivers in the same manner. It should be noted, referring to figure 4-6, that Programmable Drivers 1 through 5 and 10 differ from drivers 6, 7, 8 and 9 in that the inputs to drivers 6 through 9 are routed through an exclusive OR gate. These gates cause the test signal applied to a given driver to be inverted if the lower input leg is programmed (connected) to +5 volts in COL 54, ROWS 7 through 9. For example, connecting ROW 9, COL 54 applies a high level to the lower input of the exclusive OR gate associated with Programmable Driver number 9. This programmed high level trues the gate each time the test signal input to the second leg is at a low logic level thus, causing the input test signal to be inverted. When the OR gate is not being used as an inverter (not programmed in COL 54) the lower leg is held at a low logic level by the hold down resistor which is connected to logic ground. Output signals from the drivers are connected to the corresponding matrix ROW automatically for drivers 6 through 9. Programmable Driver outputs for ROWS 1 through 5 and 10 (if used for routing test signals) are connected to the corresponding ROW by programming columns 61 and 62 at the ROW desired. For example, the output for driver number 5 is connected to ROW 5 by programming COL 61, ROW 5 and COL 62, ROW 5 (simply punch a 5 in columns 61 and 62). Matrix ROWS 1 through 5 and 10 are dual function ROWS as noted on the right hand side of figure 4-6. In addition to being used for connecting test signals to the CARD IN TEST connector, these six ROWS can be programmed with one of four different power supply output voltages, logic ground or an external signal from connectors I1 and J2 on t he front panel. Refer to section III for programming instructions pertaining to individual ROW usage.

4-6.3 GROUP 3 STRUCTURE. Group 3 of the card reader matrix (drawing D3006) provides test signal inputs to the ten Programmable Drivers and Special Function Signal Generator (programmable elements). Columns 63 through COL 80 contain the 18 test signals generated by the "B", "C" and Special Function signal generators. Figure 3-3 illustrates the individual test signal waveforms, signal nomenclature and corresponding COL assignment. Special Function signals (+SO, +S1 and +S2) are determined by individual program requirements (if required) and drawn in the waveform chart as used. Any one of the 18 test signals is input to ROWS 1 through 10 Programmable Drivers by punching the selected ROW number into the COL containing the desired test signal. For example, to apply test signal +B3 to ROW 7, simply punch a 7 in COL 73 of the program card.

4-7 INPUT FAULT DETECTOR.

Basically, the input fault detector compares the test signal applied to the input of each Programmable Driver with the output signal from the same driver to determine if the card under test input circuit shorts the test signal to another input circuit, power or ground bus. Since a short circuit condition at a driver output (input to the card-under-test) is not reflected back to the driver input, comparison of driver input to driver output leads to detection of a shorted driver output as described below.

Each of the ten input fault circuits are identical, and the following discussion is based on the operation of ROW 1 input fault detector, shown on drawing D3003. Referring to logic diagram D3004, locate Programmable Line Driver number 1 and notice that the input test signal comes from the card reader matrix (1C80). The input test signal (determined by the program card in the card reader matrix) can be any one of 18 test signals, see paragraph 4-6.3. The test signal input (+ROW 1) is applied to 4A pin 7, inverted by B3, and routed via pin 9 (-ROW 1) to D3003 where it is input to the input fault comparator for ROW 1, 7A-12. With signal -ROW 1 on 7A pin 12 (wired to exclusive OR Al pin B) and +ROW 1 DVR (level shifted by 6A-AR2) applied to the

second input of the exclusive OR gate, both the input and output from Programmable Driver number 1 are input to the exclusive OR gate. Exclusive OR gate 7A-A1 outputs a low level each time the input signals are at the same level thus, providing a low level output if the input circuit to the card under test ('connected to ROW 1) is shorted (is not changing with the test signal input to ROW 1 Programmable Driver). With no short present, the inputs to OR gate Al are always complement signals and the gate output will remain at a high level, indicating no short.

The output signal from exclusive OR 7A-A1 is input to the "D" input of flip-flop 7A-E1. All input fault detector flip-flops are clocked by a common clock, derived from the circuits in the lower left of D3003. Input fault detector clock circuits generate a load strobe (clock) shortly after it is determined that a shorted input condition exists on the card being tested. Shorted Programmable Driver output stages could be damaged if the input test signals were not immediately removed from the driver.

The fault detector flip-flop clock circuits, located in the lower left hand corner of D3003, consist of gating control flip-flop 7A-Dl, clock/reset control gates H3 and H4, and two stage counter flip-flops M2 and M1. At the beginning of each positive going edge of +OSC (all test signals are derived from +OSC) flip-flop D1 is toggled from its reset state, providing a high level on pin E (enabling NAND gate H3) and a low level on pin F (inhibiting NAND gate H4). Gate H3, enabled with a high level on pin J, is trued each time clock signal +FREQ switches to a high level. Clock signal +FREQ switches at a 4 MHz rate providing several cycles of operation even for the fastest Card Tester test rate (1 microsecond window, see D3000). The output from NAND gate H3 is applied directly to the clock input of the two stage counter, flip-flop M2. Each positive edge of the NAND gate output clocks the two stage counter until a count of three is reached, at which time NAND gate Hi is trued (detects a count of three). Gating element HI then resets the gating control flip-flop D1 inhibiting further operation of the two stage counter and enables NAND gate H4. With NAND gate

H4 enabled, it is trued each time clock signal +FREQ reaches a high level providing a clock pulse for the fault detector flip-flops located in the center of D3003. In summary, at the beginning of +OSC clock period (positive going edge) a delay of between three and four +FREQ clock pulses (750 to 1000 nanoseconds) is provided by the two stage counter before +FREQ is gated to the input fault detector flip-flop clock inputs. After this initial delay the flip-flops are clocked by +FREQ until the next positive going edge of +OSC, at which time the clock pulses are inhibited for another 800 nanoseconds. It should be noted that all available Card Tester test signals are edge coincident with the positive going edge of clock signal +OSC and the delay generated at the beginning of the clock period allows ample time for the circuit under test input circuits to change states.

For example, if an input circuit under test is shorted, exclusive OR gate 7A-A1 will output a low level to pin B of flip-flop El, D3003. This low level is clocked into flip-flop El, after the initial delay, providing a low level on pin L of NOR gate 7A-K1 which trues the gate, is inverted by 5A-B4, trues NOR gate 5A-D3, and is inverted by 5A-D2. The low level output from inverter 5A-D2 (-INPUT FAULT) is routed to the FAULT indicator driver, lighting the indicator, and also routed to the GO flip-flop (see D3002) where it DC resets the flip-flop.

In addition, the low level output from fault detector flip-flop 7A-E1 (-ROW 1 FAULT) is output 7A pin 6 to the Programmable Driver (shown on D3004) where the low level inhibits the Card Tester test signal from the driver thus, protecting the driver from the shorted input circuit in the card-under-test. When a Programmable driver is inhibited., both of its output transistors are cut off, thereby preventing the driver from either sourcing or sinking current. The remaining nine Programmable line drivers are protected in the same manner and the fault condition is cleared by removing the shorted input and causing a Card Tester reset to occur.

4-8 PROGRAMMABLE DRIVERS.

Ten Programmable Drivers are contained in the Card Tester to convert standard TTL logic level test signals to variable test signal levels to accommodate the numerous printed circuit card families tested by the Card Tester. These

drivers provide output signal levels over the range of +24 volts for unipolar signals and 1 through 30 volts bipolar. Each driver is programmable in 100 milli-volt steps over its entire range, as controlled from the program card. All ten drivers have common power supply inputs, see D3004, on pins 47, 49 and 51, 53 for +DVR REF and -DVR REF respectively. Printed circuit cards 4A and 5A each contain five Programmable Drivers, as illustrated in the logic drawing. Inputs test signals to the drivers are connected via the card reader matrix (columns 63 through 80) and identified as +ROW (X) where (X) equals the individual ROW number associated with the driver. In the event a shorted circuit is connected through the program card to the output of the driver, the Input Fault circuits isolate the test signal from the input of the driver by trueing the -ROW (X) FAULT signal thus, inhibiting the driver input circuits. Driver outputs are routed to the card reader matrix, for connection to ROWS 1 through 10, and to the Input Fault Detector receiver circuits, for short circuit testing. Refer to paragraph 4-6.2 for detailed driver routing information pertaining to the Programmable Driver outputs and power supply reference voltages.

Programmable Drivers 6 through 9 contain exclusive OR gates at the inputs to cause the input test signal applied to these drivers to be inverted, if programmed on the program test card. Referring to D3004, driver number 6 receives a test signal from OR gate 7A-B3. Gate 7A-B3 provides a path for any of the 18 test signals connected to the input of driver 6 from the card reader matrix. For inverting the input test signal, a high level is applied to +INV 6 from the matrix (see paragraph 4-6.2) trueing the output of OR gate 7A-B3 each time the test signal switches to a low logic level. Drivers 7 through 9 operate in the same manner, as described for driver 6 above. Output signals from drivers 6 through 9 are connected directly to the corresponding card reader matrix ROW, columns 1-53 and 55.

4-9 LEVEL SHIFTER.

A Level Shifter is provided in the Card Tester to level shift the output signal (30 volts absolute, symmetrical or non-symmetrical about ground) from the

card under test to TTL circuit levels, as used in the GO/NO-GO logic circuits. The Level Shifter threshold (switching point) is controlled from the card reader matrix (see paragraph 3-5.6) by applying various voltages, and combinations of voltages, to the four resistive inputs to the Level Shifter, as shown in the center left hand side of D3008. As shown in the drawing, the four resistor inputs are wired to the +V, -V and +5 volt power supplies and commoned at the (-) input of the Level Shifter. The (+) input is connected directly to the circuit under test output pin selector switches on the Card Tester from panel. As each card under test output pin is selected, the output signal is routed directly into the (+) input of the Level Shifter. The Level Shifter switches as the input signal (applied to the (+) input, 6A-ll) crosses the programmed threshold. In essence, the Level Shifter switches at approximately one-half the algebraic value of the voltage(s) to the resistors at the (-) input (AR11 pin 3). Output signals from the Level Shifter (shifted to TTL levels) are routed to the GO/NO-GO logic Edge Detector (+LS INPUT PIN) which detects each transition in the wavetrain, see D3002. Locate 2A-24, upper left hand corner of D3002, and note the output from Level Shifter 6A-ARll (+LS INPUT PIN) as it is applied to the Edge Detector circuits. The output from inverter 2A-Hl is applied to flip-flop C4 (see paragraph 4-10.1) and also to inverter 3A-L1 by way of 2A-21 and 3A-39. Inverter 3A-L1 inverts the negative signal back to a positive signal which is output to test point IN/OUT PIN IC (TP1l8 shown on D3008) for circuit under test output signal monitoring by the operator/technician. Test point 1 (IN/OUT PIN DIRECT), also shown on D3008, provides the input signal to the Level Shifter at the front panel for monitoring purposes. Both TP1 and TP18 are located on the Card Tester front panel to the left of the POWER ON indicator, directly above the GRD test point.

4-10 GO/NO-GO OPERATION.

Basically the GO/NO-GO logic (hereafter referred to as Test Logic) consists of an Edge Detector/Counter, Bit Counter, GO flip-flop, NO-GO flip-flop and end-of-frame no-go detector. These circuits are used in conjunction with the edge and bit count switches (WAVEFORM TEST switches A and B) to compare

the time interval between distinct edges (transitions) of the output signal of the circuit under test. This measurement provides a concise indication as to whether or not the circuit under evaluation is functioning according to design requirements. Detailed descriptions of the above mentioned functional circuits are provided in subsequent paragraphs.

The overall concept of the GO/NO-GO logic operation is that when testing digital circuits, the circuit under test will produce outputs in response to its inputs (provided by the Card Tester) in a predictable, logical fashion. Before analyzing the circuit operation, the terminology used in the timing must be defined and kept in mind:

(1) Frame: A frame is the period of the slowest-changing test signal generated by the Card Tester, e.g., one complete cycle of B7.

(2) Bit: The frame is divided into 512 bit periods and a bit is the shortest interval between transition of any test signal with respect to any other test signal, e.g., from a positive edge of BO to the next positive edge of CO.

Since the test signal transitions are coincident either with "B" time (BO-B7) or "C" time (CO-C6) a transition or change-of-state can be applied to the circuit-under-test only at "B" time or "C" time, and the circu it will produce a change-of-state only in response to a "B" time or "C" time test signal after propagating through the circuit-under-test. The test rate must be selected by the programmer to ensure that the bit period is long enough for the circuit-under-test to propagate before the beginning of the next bit period.

In the Card Tester, the/GO/NO-GO logic is implemented by sampling the output of the circuit-under-test each bit time to determine if the circuit-undertest produced a change-of-state (edge). Edges thus detected are counted beginning with each frame. Also, bit periods are counted, in a separate counter, beginning with each frame. During operation of the Card Tester, the operator selects a specific edge on the front panel "A" switch and the bit period in which that edge

is expected to occur on the "B" switch. Then, if the selected edge occurs at the correct bit time a GO condition results. On the other hand, if the circuit-under-test malfunctions and produces a logical error, causing the selected edge to occur during any bit time other than that selected, a NO-GO condition results.

4-10.1 EDGE DETECTOR OPERATION. The Edge Detector provides an output pulse for each transition detected in the card under test output signal selected by the IN/OUT SELECTOR switches. These edges are counted by the Edge Counter, see paragraph 4-10.2, which is strobed (clocked) by the Edge Detector output pulses. Referring to D3002, locate the Edge Detector in the upper left hand corner, printed circuit card 2A, and note that the input pin receives the card under test output signal from the Level Shifter, see paragraph 4-9. Flip-flops C3 and C4 (printed circuit card 2A) are connected as a shift register and are strobed at the bit rate by -OSC. Both flip-flop outputs are connected to the input of exclusive OR gate A4 which functions as a comparator to the two flip-flops. Each time both flip-flop outputs are equal, OR gate A4 outputs a low level and each time the outputs are opposite resulting from a level change from the circuit-under-test being shifted into 2A-C4, OR gate A4 outputs a high level which enables NAND gate J2. Once enabled, NAND gate J2 is trued when +OSC and +2 OSC are at a high level thus, producing a low level pulse for the duration of one-half a cycle of +2 OSC. The low level output Dulse from NAND gate J2 is connected directly to the Edge Counter clock input pin, 3A-250 Each time an output signal under test changes states the Edge Counter is incremented by one, as illustrated in figure 4-7. As shown in the timing diagram, the signal being tested is located about midpoint in the diagram and the corresponding Edge Detector clock output (+ EDGE COUNTER CLOCK, 2A-42) is shown two lines below the output signal. With respect to the output signal and beginning of frame time, the Edge Counter is reset at the beginning of the frame and clocked each time the +EDGE COUNTER CLOCK pulse goes to a low logic level, indicated by the arrow on each pulse. Edge Counter operation is delineated in paragraph 4-10.2.

4-10.2 EDGE COUNTER'OPERATION. Output signals from the card under test are tested by measuring the distance from the start of a frame to each transition in the output signal as it occurs. Each of these transitions are detected by the Edge Detector and counted by the Edge Counter to provide a means of identifying individual edges for measurement. WAVEFORM TEST switch A is wired such that a binary count corresponding to the switch position is applied to the compare circuit located under the Edge Counter on D3002. As shown, -EDGE 1, 2, 4, and 8 are input to the comparator from the left side of the logic drawing, from S5 (switch A). Each of the outputs stages from the four stage Edge Counter are applied to the comparator and as the counter increments from its initial reset condition, it will cause a compare output when the accumulated count reaches the switch setting number. Once the counter reaches the switch setting value, AND gate 3A-K1 (pin F) outputs a high level (is trued) enabling AND gate A4. AND gate A4 is trued on the next high level -OSC output producing a positive edge compare pulse (+EDGE CMPR). Edge compare pulse (+EDGE CMPR) clocks the Edge Compare Reset Flip-flop, in turn resetting the Edge Counter; clocks the GO Flip-Flop, loading either a Bit Counter compare or non-compare; clocks the NO-GO Flip-Flop, loading either a Bit Counter compare or non-compare; and is applied to the Self Test logic circuits to clock flip-flop IA-Dl in test position 4 (see D3008). Once the Edge Compare Reset Flip-flop is clocked (clocked by +EDGE CMPR), output pin E remains at a high level until the beginning of the next frame. A high level on pin E (flip-flop 3A-B1) holds the Bit Counter reset until the beginning of the next frame at which time the flip-flop is DC reset (causing output pin E to change to a low level) by -FR START. In summary, it has been shown that for each setting of WAVEFORM TEST switch A, a +EDGE CMPR pulse is generated as the Edge Counter is incremented to a count equal to the selected value. In this manner each transition in the card under test output signal is uniquely identified with respect to the beginning of the frame of the Card Tester. As a compare is made, both the GO and NO-GO flip-flops are

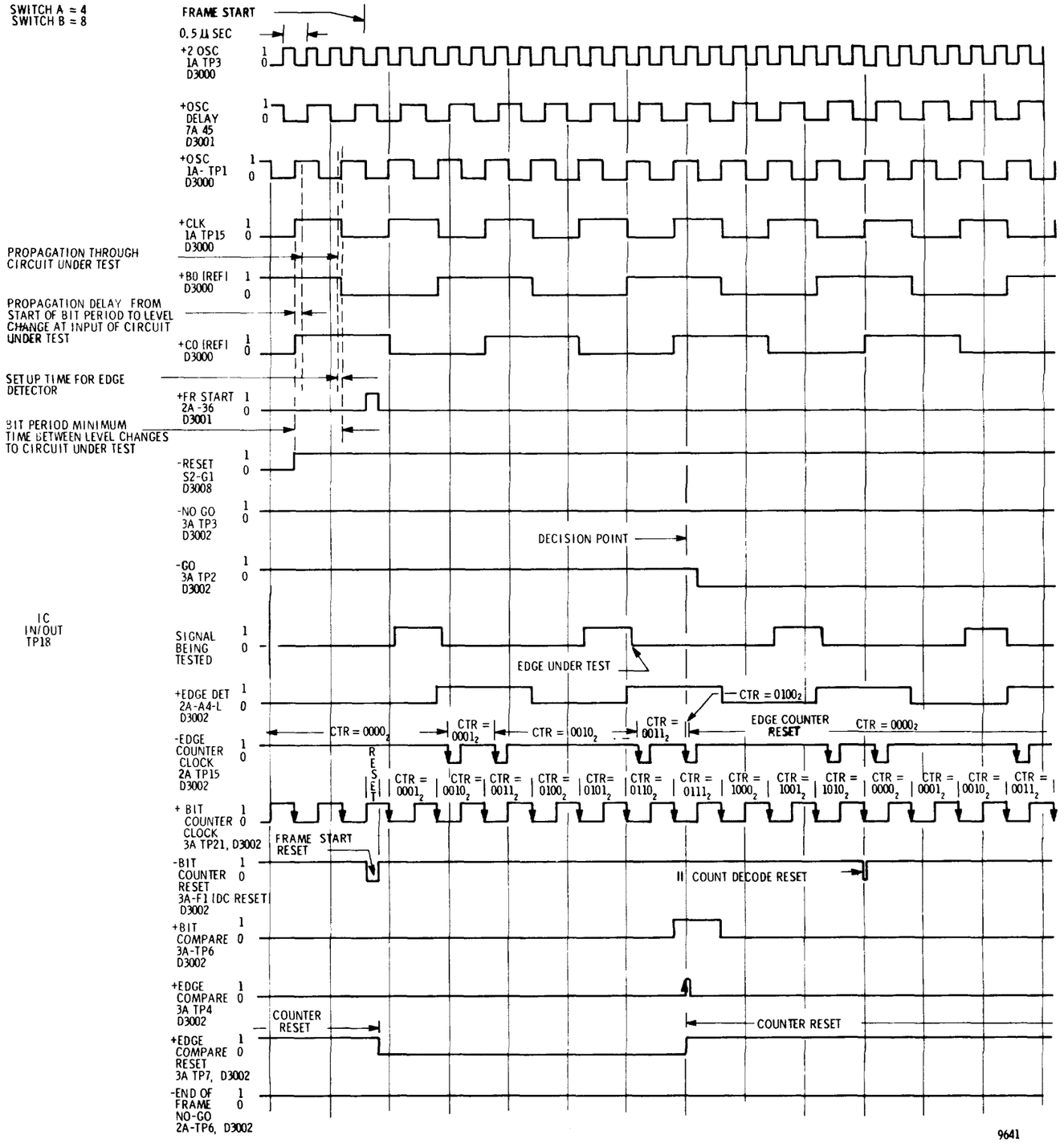


Figure 4-7. ICT 102 Timing Diagram

strobed by the compare output pulse to load either a GO or NO-GO test indication, see paragraph 4-10.5 for detailed operation.

4-10.3 BIT COUNTER RATE SELECTION. Bit Counter operation is controlled from a quad gating element, shown in the lower left corner of D3002, which provides four separate Bit Counter clock inputs, as determined by the program card. Clock inputs +OSC, +CLK, +B0, and +B1 are applied to gate 3A-E1 to advance the bit counter at the bit rate, 1/2 the bit rate, 1/4 the bit rate, or 1/8 the bit rate. For most testing situations, OSC is selected by the programmer to clock the Bit Counter at the bit rate (+BIT OSC is programmed to clock signal +OSC into the Bit Counter). Each of the remaining three clock rates is used mainly for testing asynchronous circuits such as single shots. For testing single-shots, Bit Counter outputs must be determined which accommodate the variable (asynchronous) timing of the trailing edge from the single shot under test to ensure that the asynchronous edge falls within a specific count of the bit counter. Refer to paragraph 3-5.2 for detailed programming instructions for expanding the Bit Counter clock period. It should b e noted that pull-down resistors are provided at the four card reader matrix inputs to the quad gating element which inhibit the gates not programmed. In selecting an input, the card reader matrix connects the programmed input to +5 volts causing the input to swing to a high logic level, enabling the selected gate.

4-10 4 BIT COUNTER OPERATION. The Bit Counter, shown in the lower center of D3002, provides unique time periods within which the card under test output signal transitions can occur. The Bit Counter recycles after the count of ten (resets to zero providing an 11:1 count) to provide a reasonable minimum probability of the selected edge occurring at a bit period which is an exact multiple of the desired bit count. It is likely in many cases that more than 11 bit periods can occur between successive edges from the circuit-under-test output signal. This being likely, if an edge does not occur within 11 bit periods, the Bit Counter recycles and continues to count. Since most printed circuit card families being tested by the Card Tester involve number systems with a radix of 2 or 10,

and the smallest possible multiple of 11 which is divisible by a power of either 2 or 10 is 110, there is little likelihood of a circuit-under-test malfunctioning in such a manner as to produce the selected edge count coincident with the selected bit count which is not the desired number of bit periods following the previous edge.

The four stage Bit Counter, 3A-F1 on D3002, is initially reset at the beginning of the frame, -FR START input through OR gate L3 pin N, and automatically reset after the count of 10 by NAND gate L2. Gate L2 decodes a count of 10112 and is immediately DC reset to zero through gate L3, input legs A and B. Once reset to zero, from decoded count eleven, the decoder output (3A-L2 pin H) changes to a high level, removing the reset input to OR gate L3. Four outputs from the Bit Counter are compared with the switch setting of WAVEFORM TEST switch B (input to the compare circuits from the lower left hand corner of D3002) to provide a high level compare pulse output from AND gate K2 each time the Bit Counter reaches the predetermined counter value. This high level output, K2 pin H, is applied to the "D" input of the GO and NO-GO flip-flops, 3A-G1 and G2, respectively. In summary, as the Bit Counter recycles from zero through ten (0000_2 through 1010_2) AND gate K2 outputs a high level when its count compares with the switch setting of WVAVEFORM TEST switch B, switch S4. If the selected circuit-under-test transition occurs during the selected bit period, the GO and NO-GO flip-flops are set, as explained in paragraph 4-10.5.

4-10.5 GO/NO-GO FLIP-FLOP OPERATION. Both the GO and NO-GO flip-flops are clocked by the edge compare output pulse, +EDGE CMPR, to load the Bit Counter comparator output level into the flip-flops thus, storing the result of the time measurement performed on the circuit-under-test output signal for the WAVEFORM TEST switch settings on switches A and B. Four individual conditions can occur within a frame for each test performed on the output signal from the circuit-under-test, as listed below:

a. GO Indication If both the Edge Counter compare and Bit Counter compare occur at the proper time, the GO and NO-GO flip-flops are set indicating

a properly located output edge has been tested.

b. NO-GO Indicated (due to improper Bit Counter count) If the transition under test is detected and the Bit Counter is not at the required count, the GO and NO-GO flip-flops are reset indicating that an output transition did occur but, at the wrong time period (as indicated by an non-compare from the Bit Counter compare circuits).

c. NO-GO Indicated (due to lack of Edge Counter compare) If the output signal from the circuit-under-test does not change levels for a complete frame (or does not reach the selected Edge Counter count) an End-Of-Frame NOGO is generated which DC resets the NO-GO flip-flop indicating a NO-GO condition.

d. Input Fault Override Any time an input fault condition occurs, the GO flip-flop is held DC reset until the cause of the input fault malfunction has been eliminated. Refer to paragraph 4-7 for a detailed discussion of the Input Fault Detector operation.

GO flip-flop 3A-G1 is DC reset each time + GO OVRIDE (upper right hand corner of D3002) is trued, high level output. NOR gate 2A-J3 is trued under the following conditions:

a. When any of the front panel switches are pressed or rotated from one position to another, -RESET is trued causing NOR gate J3 to change to a high level which is inverted by 4A-D2 and applied to the DC reset input of GO flip-flop G1.

b. -INPUT FAULT is trued each time a shorted input line to the card under test is detected by the Input Fault Detector. With -INPUT FAULT at a low level, the GO flip-flop is held DC reset.

c. -NO-GO provides a DC reset for the GO flip-flop when ever a NO-GO condition is detected.

The GO flip-flop is clocked by +EDGE CMPR once each frame, as determined by the WAVEFORM TEST switch A setting and the occurrence of a valid output from the signal under test. A high level into G1 pin B ("D" input of flip

flop) is loaded with +EDGE CMPR causing output G1 pin F to be trued (-GO is at a low level). Signal -GO inhibits the End-Of-Frame NO-GO Detector (2A-39 at a low level) and also lights the GO indicator (-GO is switched to lamp driver 1A-C4 on D3003 by S3 in positions 1 through 6, see D3008) shown on D3008, located in the lower right hand corner.

The NO-GO flip-flop operates in the same manner as the GO flip-flop, described above, except the output is taken off the "Q" output of the flip-flop instead of the "Q" output. Signal +EDGE CMPR clocks flip-flop 3A-G1 causing the compare output from the Bit Counter to be loaded as the correct output signal transition is detected. If the Bit Counter compare output is at a low level (indicating an invalid output transition window) this low level is loaded into flip-flop G2, causing G2 pin J to change to a low level indicating a NO-GO condition. Trueing -NO-GO causes the NO-GO flip-flop to latch itself in the true state through NOR gate 3A-A3. Once latched, the NO-GO flip-flop remains latched until -CLEAR is generated (clearing the flip-flop by DC setting input G2 pin K) from Delay Reset Flip-Flop 3A-H2, located at the top of the drawing directly above the NO-GO flip-flop. The Delay Reset Flip-Flop ensures that at least 64 milliseconds elapse after any of the front panel switches have been pressed or rotated. Delay reset signal -CLEAR holds the Edge Counter reset as well as the End-Of-Frame Detector Flip-Flop and the NO-GO Flip-Flop for a period of approximately 64 milliseconds after each switch generated reset.

End-Of-Frame NO-GO Detector operation is based on the outcome of the GO and NO-GO flip-flop operation throughout a frame period. EOF Detector circuits are located in the lower right hand corner of D3002 and are enabled at the beginning of the frame, for a one frame period, by +EOF DET input on pin 2A-35. Signal +EOF DET is generated by flip-flop 3A-H1 (EOF Detector Flip-Flop) in the following sequence. Flip-flop HI is held DC reset (-CLEAR input to pin A) for 64 milliseconds after a system reset causing +EOF DET to remain at a low level until the trailing edge of the first -FRAME START pulse, input to the clock input pin C. At the trailing edge of -FRAME START, flip-flop HI, pin E toggles to a

high level and remains at a high level until the trailing edge of the next -FRAME START pulse (for a one frame period), enabling NAND gate 2A-D2 (input pin 35). NAND gate 2A-D2 is trued only for the duration of the -FRAME START pulse at the beginning of the second frame after a system delay reset has taken place. During the frame start pulse width, of the second frame, NAND gate 2A-E2 is enabled and will be trued only if NAND gate 2A-D3 is trued. Both inputs to NAND gate D3 must be at a high level to cause the output to swing low, trueing gate E2. As shown in logic drawing D3002, input pins.2A-37 and 39 are tied to -NO-GO and -GO respectively and are both at a high level only when neither a GO or NO-GO have been generated. To summarize, the EOF NO-GO Detector is enabled for the pulse duration of -FRAME START (for the second frame after a system reset) which trues the detector only if the GO and NO-GO flip-flops have not detected either test condition. Once trued, -EOF NO-GO is routed out 2A-Gl (pin 20); in pin 10 of card 3A; to pin I of OR gate A3 which in turn trues the OR gate (3A-A3) causing -NO-GO to be trued from the DC reset on flip-flop G2. Thus, if no decision has been made as to the validity of the output signal under test after a period of one frame, the EOF NO-GO Detector forces the NO-GO flip-flop to output a NO-GO indication which lights the NO-GO indicator located on the front panel.

4-11 SELF TEST LOGIC OPERATION. Self Test logic circuits are provided, see lower portion of D3005, to allow the operator to rapidly verify the Card Tester operation by exercising the majority of the internal functional circuits described in the preceding paragraphs. Operating procedures used to initialize the Card Tester self test circuits are delineated in paragraph 3-3. All control circuits required to initiate Self Test operation are provided by the automatic self test program card (IBM tabulating card), front panel switch S3 (IN/OUT SELECTOR TENS switch positions TEST 1 through 4) and the two flip-flop circuits shown in drawing D3005. Each input and output pin associated with the two flip-flops are wired directly to various positions of S3, as depicted in D3005. Actual switch wiring information associated with the automatic self test circuit's

and S3 is shown on D3008 (center portion of wiring diagram). The simplified switch diagrams shown on D3005 are illustrated in this manner to aid the reader in understanding Self Test circuit operation. Each of the four switch positions (SELF TEST 1 through 4) are described in the following paragraphs. Additional Self Test Capabilities (Self Test programs A and B) are described in paragraph 4-11.5.

4-11.1 TEST POSITION 1. Test position 1 checks the Card Tester basic oscillator and Self Test flip-flops by holding the flip flops in a reset state with the reset push-button on the front panel and then allowing the flip-flops to toggle, as the reset switch is released. Basic clock signal +FREQ is used to clock the Self Test flip-flops after the reset switch is released causing the GO indicator to light and the NO-GO indicator to extinguish.

Referring to D3005, note that the DC reset lines to each Self Test flip-flop, 1A-D1 and D2, are wired to -CLEAR which is generated each time the NO-GO indicator (reset push-button) is pressed (or rotary switch is changed to another position) for a period of approximately 64 milliseconds after the push-button is released. While -CLEAR is low (true) flip-flop D1 outputs a high level on pin 44 (-GO SELF TEST is not trued) and flip-flop D2 outputs a low level on pin 43 (-NO-GO SELF TEST is trued), lighting the NO-GO indicator on the front panel. Refer to figure 4-8 for a timing diagram representation for test 1 operational characteristics. As shown in the timing diagram, the GO indicator is OFF and the NO-GO indicator is ON while the reset push-button is pressed and at the first positive edge of -FREQ, after -CLEAR changes to a high level, the GO indicator lights and the NO-GO indicator extinguishes. Self Test flip-flop 1A-D1 is clocked by the positive going edge of +FREQ, toggling output pin E to a high level which in turn clocks flip-flop 1A-D2 (changing -NO-GO to a high level). Figure 4-10 illustrates the Automatic Self Test program card.

4-11.2 TEST POSITION 2. Self Test position 2 provides a check on the operation of clock signal +2 OSC and "B" test signal generator by utilizing test signal +B7 to toggle the Self Test flip-flops while the Card Tester is operating

at a slow Test Rate. When the Card Tester is switched to TEST position 2 (switch S3) the GO indicator switches ON and OFF for a period of 4.2 seconds in each state and the NO-GO indicator remains OFF. Operation of the Self Test flip-flops for TEST position is illustrated in figure 4-8 (timing diagram). Test position 2 connects (see D3005) +2 OSC clock signal into the clock input of flip-flop 1A-D1 which causes the flip-flop to toggle each time the "D" input signal changes. The "D" input to flip-flop D1 (in TEST 2) is +B7 which is operating at the slowest Test Rate (BO operating at 15.25 Hz). If the "B" Test Signal Generator is operating correctly, +B7 will be at a high level for a period of 4.2 seconds and then switch to a low level for a period of 4.2 seconds. Output pin F (flip-flop 1A-D1) will change states on the positive edge of +2 OSC following a change in test signal +B7, as indicated in timing diagram figure 4-8. Self Test flip-flop D2 (generates -NO-GO) is clocked by the output from flip-flop D1 but, does not light the NO GO indicator because S3 switches +5 volts (high logic level) to the "D" input in TEST position 2.

Note

Initially (for the duration of the first frame up to approximately 8.39 seconds), the NO-GO indicator can be illuminated. This condition is normal, as it is impossible to determine when the operator changes the TEST switch to position 2, with respect to the state of +B7. Self Test flip-flop D2 sets a high level (extinguishing the NO-GO indicator) into storage as the output from D1 (D1 pin E) changes to a high level. This change in D1 could occur any

where from a few microseconds up to as long as 8.39 seconds after switching to position TEST 2 (after -CLEAR switches to a high level).

4-11.3 TEST POSITION 3. Test position 3 provides a functional test for the frame start strobe (which further verifies the operation of the "B" Signal Generator) and Test Signal +C5, which checks the operation of the "C" Signal Generator. To operate the Card Tester in TEST 3, the operator simply places the IN/OUT SELECTOR TENS switch (S3) to TEST position 3 and observes the TEST indicators. TEST indicator GO should blink ON and OFF at a rate of 4.2 seconds in each state. The TEST NO-GO indicator should remain OFF for the duration of the test. Initially, however, the NO-GO indicator can be lit for a period from a few milliseconds (could not be observed by the human eye) up to 8.39 seconds, depending on the time that the initial reset delay (-CLEAR) is removed from the DC reset inputs of the Self Test flip-flops.

Referring to D3005, it is shown that Self Test flip-flop 1A-D1 is clocked by +B7 (switch S3 inputs +B7 into PC card 1A pin 47 when positioned in TEST 3) which occurs in the center of each frame. Flip-flop D1 output pin F is connected to the TEST GO lamp driver by section G of S3 when S3 is positioned in TEST position 3. Signal -FR START (occurs at the beginning of the frame) is applied to the DC SET input of D1 causing the flip-flop to be toggled (GO indicator turns OFF) at the beginning of each frame. It should be noted that the Self Test program card operates the Card Tester at the slowest test rate providing a frame duration of approximately 8.4 seconds. The output from flip-flop D1 (pin E) is routed directly into the clock input of flip-flop D2, causing D2 to be loaded with a high level (+C5) each time the clock input changes to a high level. Outputs from the two Self Test flip-flops are routed through other sections of S3 to the TEST lamp drivers.

4-11.4 TEST POSITION 4. Self Test position 4 checks the operation of the

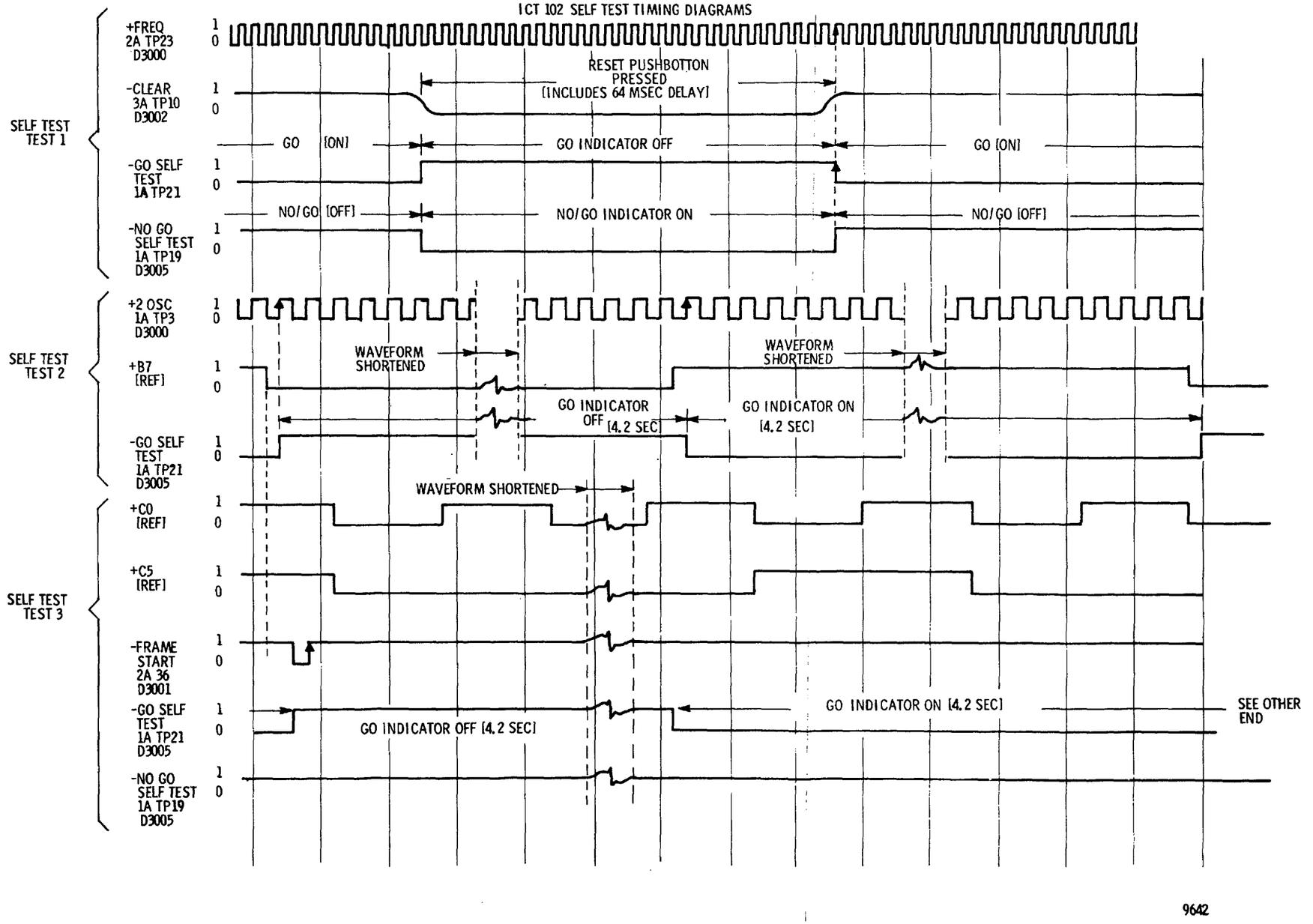
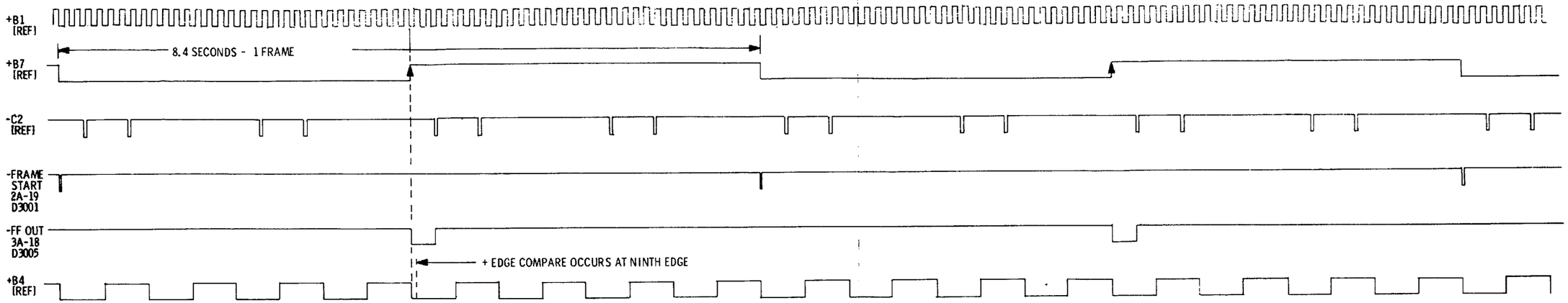


Figure 4-8. Self Test 1 through 3 Timing Diagram



NOTE:

1. TEST 4 APPLIES TEST SIGNAL +B4 TO EDGE DETECTOR.
2. SET SWITCH A TO 9.
3. SET SWITCH B TO 7.

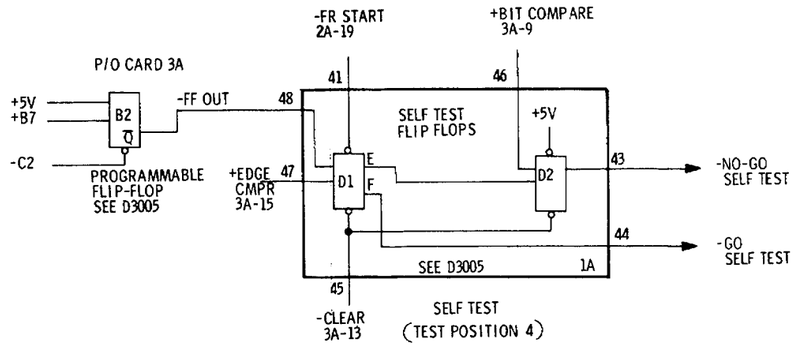


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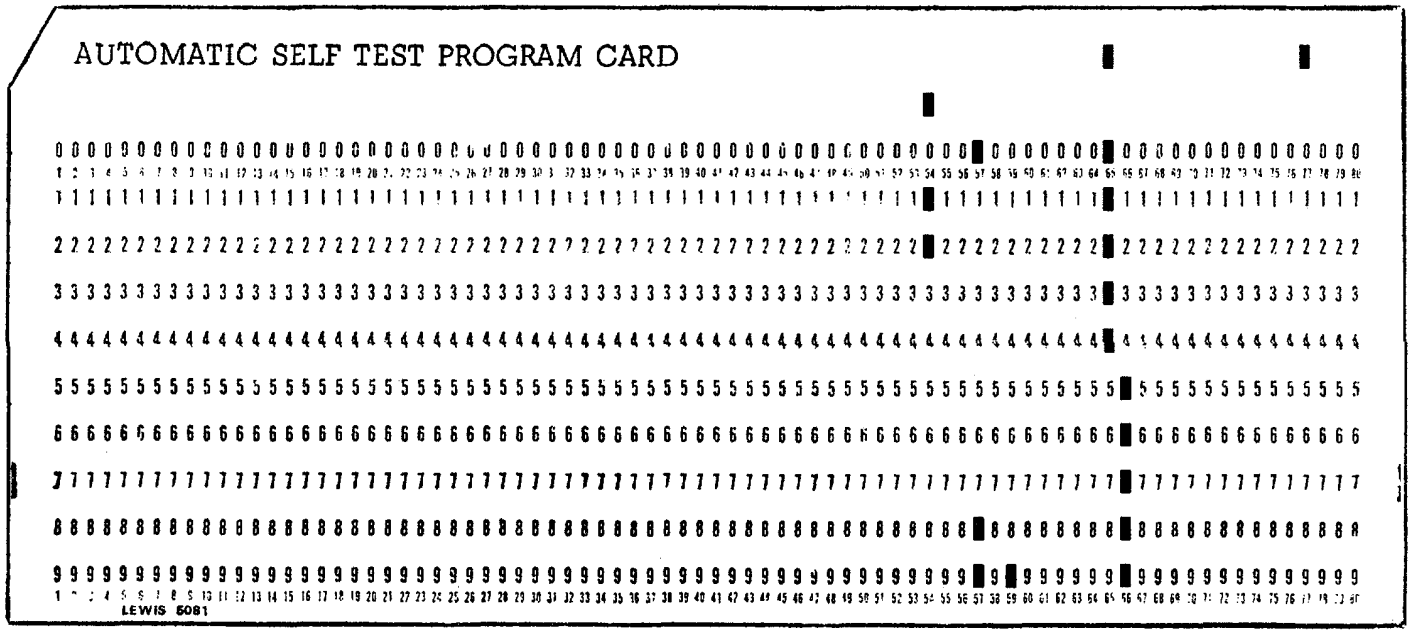
Figure 4-9. Self Test Position 4 Timing Diagram

GO/NO-GO test circuits in the Card Tester by applying, via section A, position 10 of S3 (shown on D3008) +B4 to the Edge Detector to cause +EDGE CMPR to load a low level into the Self Test flip-flop, LA-D1 (see figure 4-9 for a simplified illustration of the Self Test circuits connected for TEST position 4). In TEST position 4th GO indicator flashes ON and OFF for approximately 8.4 seconds in each state. The NO-GO indicator remains in the OFF position throughout the test unless there is a malfunction in the Bit Counter. Troubleshooting information determined from the symptoms uncovered in Self Test operations are delineated in section V of this manual. Figure 4-10 illustrates the Automatic Self Test program card.

Referring to figure 4-9, it can be seen that programmable flip-flop B2 is programmed such that test signal +B7 is applied to the clock input and -C2 is programmed to the DC reset input. The Q output from flip-flop B2 is routed to the "D" input of Self Test flip-flop D1, see -FF OUT shown in the timing diagram above the test flip-flops. Signal -FF OUT changes to a low level on the positive edge of +B7 and is pulled high again at the first negative pulse of -C5 after the positive edge of +B7. The time duration between negative going edges of -FF OUT is approximately 8.4 seconds. As shown in the simplified drawing, figure 4-9, flip-flop 1A-D1 is clocked by +EDGE CMPR which occurs shortly after the ninth edge of test signal +B4 causing a low level to be loaded into flip-flop D1, turning OFF the TEST GO indicator. With flip-flop D1, pin E at a low level flip-flop D2 will be clocked when D1 pin E changes to a high level. At -FR START time of the next frame (midpoint between the two positive going edges of +B7 in the timing diagram) flip-flop D1 (pin E) is pulled high by the DC SET input pulse (-FR START) turning the GO indicator ON and loading flip-flop D2 with the Bit Counter output which, in this case, should be at a high level, assuming that the Bit Counter is functioning and WAVEFORM TEST switch B is positioned at 7. Once clocked, the output from flip-flop D2 turns the NO-GO indicator OFF and keeps it off as long as the Card Tester is operating in TEST 4.



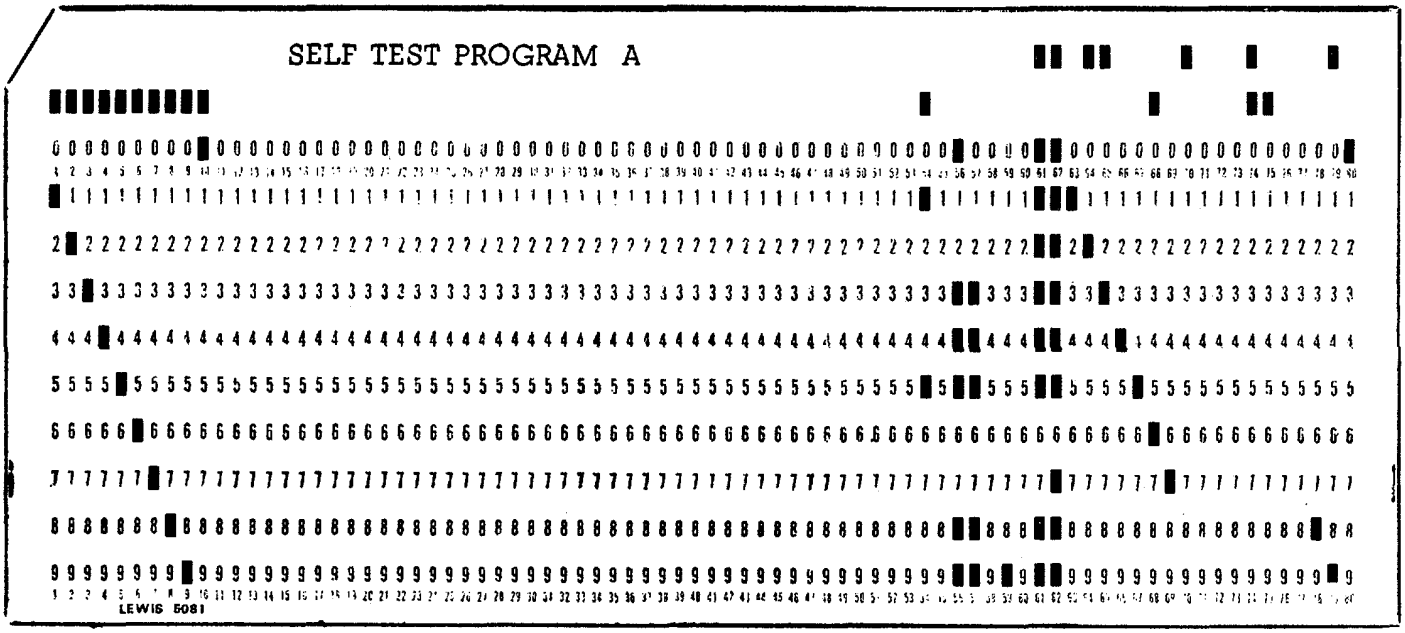


Figure 4-10. Self Test Program Cards

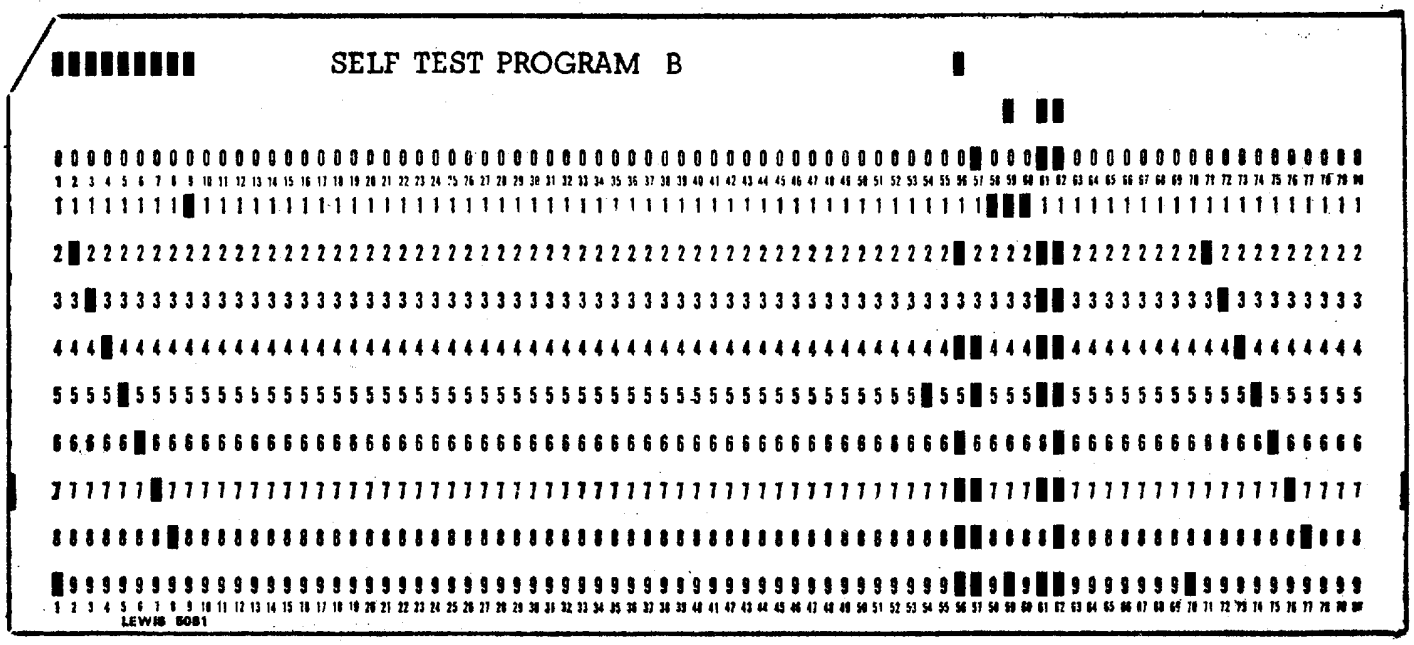


Figure 4-10 (Cont'd) Self Test Program Cards

4-11.5 TEST SIGNAL SELF TEST OPERATION. Additional Self Test verification of internal circuit operation is provided by Self Test programs A and B. Program A routes all "C" clock test signals and "S" clock signals through the programmable drivers to the CARD IN TEST connector to be selected by the operator and individually tested according to the information presented in section III, paragraph 3-3. All testing functions performed by program tests A and B are under program control and require no special circuits or Card Tester wiring. Figure 4-10 illustrates the A and B test program cards.

4-12 LOADS FOR CIRCUITS UNDER TEST.

Programmable load resistors are available at the CARD IN TEST connector pins for loading the output circuits of the card-in-test. These resistors are connected to the output pins by the card reader matrix and individual program card for each card to be tested. Drawing D3005 shows the two resistor printed circuit cards, upper left hand corner, and the voltages available at the

common input to each board. For example, load resistor PC board 9A contains 54 resistors which are commoned and connected to +5 volts, 9A pin 56. Load resistor board 8A also contains 54 resistors which are commoned but, the common side of the resistors are connected to LOAD REF which is wired to the card reader matrix. LOAD REF can be connected, under program control, to +5 volts, +V power supply output, -V power supply output, +V power supply output voltage and logic ground to provide a diversified selection of reference voltages to accommodate the many printed circuit card families tested by the Card Tester. Additional flexibility is provided for testing families with unique output loading characteristics by inserting load resistor PC boards with other resistor values to accommodate these special load characteristics. The individual load resistors are wired directly to the corresponding card reader COL numbers associated with the CARD IN TEST connector pins. Card 8A and 9A are wired to ROWS 12 and 11 of the card reader matrix, respectively. Refer to paragraph 3-5.12 for load resistor programming information, which includes reference voltage programming and CARD IN TEST connector output pin loading information.

4-13 POWER SUPPLY THEORY OF OPERATION.

All internal power supply voltages required for Card Tester operation and the testing of printed circuit boards are generated in the single power supply located along the rear panel of the Card Tester. This power supply operates from a single phase 115 volt AC power source and provides the following DC voltages:

a. -6 VDC Used for internal Card Tester circuits.

b. +12 VDC Used for internal Card Tester circuits with separate fused output for indicator lamps located on the front panel.

c. +5 VDC EXT Adjustable +5 volt output (+4.5 to +5.5 volts) used for supplying logic voltages to the card-under-test via the CARD IN TEST connector, pin 54. This voltage can also be connected to any of the remaining 54 programmable pins on the CARD IN TEST connector.

d. +5 VDC INT Supplies power for internal Card Tester logic circuits contained on printed circuit cards. Using separate voltages for internal

logic circuits eliminates erratic Card Tester operation due to faulty circuits on cards-under-test.

e. Programmable Power Supplies Three program controlled power supplies which are controlled by the program test card to output from 500 millivolts to 26.1 volts for the +V and -V power supplies and from 1.0 volt to 26.1 volts (either positive or negative output polarity) for the +V power supply.

The following paragraphs provide the detailed theory of operation descriptions for the internal power supply circuits.

4-13.1 PRIMARY VOLTAGE SURGE PROTECTION. Primary voltage surge protection is provided by the THERMOTAB triac and associated circuit shown in the upper left hand corner of D2990, located in section VII. Under normal input voltage conditions the triac is gated OFF and appears as an open circuit. As the input voltage increases to approximately 210 volts peak the triac is gated ON by the voltage developed across R69 and R70 and the neutral and high side of the AC input voltage are connected through R71, a 4.7 ohm resistor, causing fuse F1 to open. With fuse F1 open the power supply circuits are protected from further increase in the primary AC voltage.

4-13.2 +12 VOLT POWER SUPPLY. The +12 volt power supply operates as a full-wave center tap power supply utilizing an emitter follower regulator with Zenered base reference control. Approximately 400 milliamperes of current is provided by the +12 volt power supply and distributed as follows:

a. Indicator Lamps: 320 milliamperes

b. Internal Card Tester Logic: 50 milliamperes Input transformer T1 develops 24 volts RMS across terminals E6 and E7 (red wires) which is full-wave rectified by diodes CR1 and CR2 to provide approximately 15 volts at the cathode of the diodes, see D2990. Zener diode VR3 develops a regulated +13 volts at the base of transistor Q4 which operates as an emitter follower regulator for the +12 volt power supply. The emitter junction of transistor Q4 follows the base voltage (minus approximately 700 millivolts base-emitter drop) providing a regulated output voltage of approximately

+12.3 volts. Filtering for the output voltage is developed by capacitors C1 and C2. It should be noted that the +12 volt lamp output is protected with a 3/4 ampere fuse (F1).

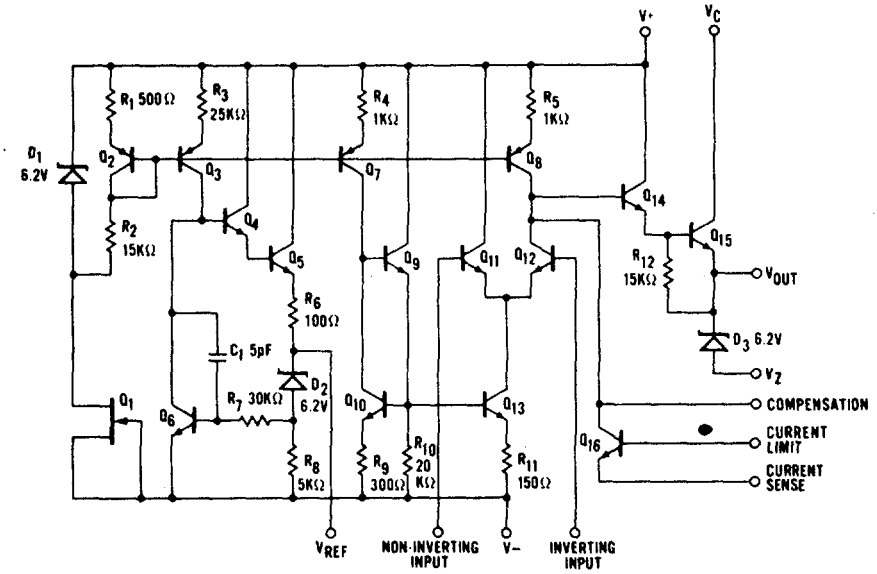
4-13.3 -6 VOLT POWER SUPPLY. The -6 volt power supply operates in the same manner as the +12 volt power supply (para 4-13.2) except that the DC voltage is developed across a full-wave bridge rectifier instead of a fullwave center tap rectifier. Referring to D2990, 15 volts RMS is developed across T1 secondary terminals E8 and E10 which is rectified by diodes CR3 through CR6, connected as a full-wave bridge rectifier. Zener diode VR4 regulates the base voltage of emitter follower regulator Q5 at -6.8 volts. With transistor Q5 connected as an emitter follower, the emitter junction of the transistor follows the base bias voltage developing a regulated output voltage at -6.0 volts. Capacitor C9 filters the output voltage which is available at pin 26 of the output connector, P1. Input filtering is provided by capacitor C10 which is connected to the collector of Q5. The -6 volt power supply provides approximately 200 milliamperes to the internal Card Tester logic circuits.

4-13.4 +5 VOLT POWER SUPPLIES, Both the internal (INT) and external (EXT) +5 volt power supplies operate in the same manner. Refer to paragraph 1-3.8.1 for general power supply usage within the Card Tester. Drawing D2990 should be referenced for the following power supply operation description which is directed towards the +5 volt INT power supply. Emitter follower regulation is incorporated in the +5 volt power supply, as in the +12 volt and -6 volt power supplies, but, this power supply utilizes a precision voltage regulator to control the reference voltage for the transistor base instead of the fixed reference generated across the zener diode. The precision voltage regulator also provides current limiting (automatically resets to normal state when short is removed) and crowbar overvoltage protection. The following general characteristics for the precision voltage regulator (AR1 through ARS) are provided as an aid in understanding the power supply operational characteristics.

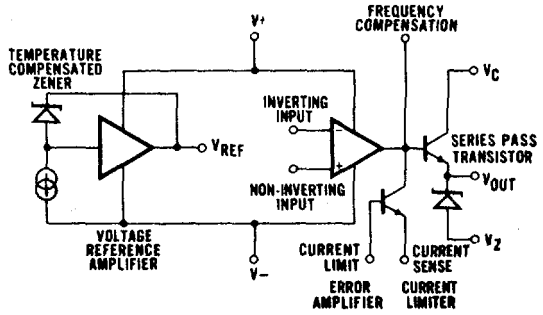
a. Part Number: Fairchild U5R7723393 (u723)

b. Absolute Maximum Ratings:
   1. Pulse voltage from V+ to V(50msec) 50 volts
   2. Continuous voltage from V+ to V40 volts

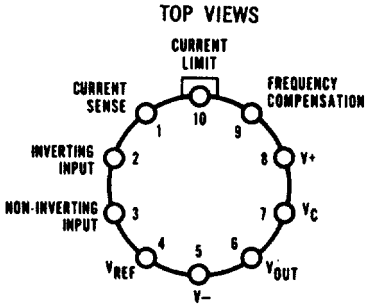
c. Schematic Diagram:



d. Equivalent Circuit:



e. Connection Diagram



Note
Pin 5 connects to case.

f. Output Voltage Range: Adjustable from 2 through 37 volts.

Referring to D2990, the output of AR1 (pin 6) controls the base bias for series pass transistor Q3. Regulator AR1 outputs a V REF voltage of typically +7.15 volts which is divided across resistors R5, R2 and R3 to develop the adjustable range. Adjustment of R2 provides an output voltage range of approximately 4.5 to 5.5 volts. Current limiting is controlled from resistor R60. When the series regulator current exceeds approximately 1200 milliamperes, the voltage developed across R60 lowers the drive current available from AR1 to cut off Q3. Resistor R5 is used to protect the current limit sensing circuit internal to AR1. Overvoltage protection consists of the crowbar network Q1 and VR1 which clamps the output voltage to ground if the output seeks a voltage greater than +7.0 volts. Zener diode VR1 (V_z = 5.6 volts) holds the gate of thyristor at -0.4 volts when the output of the power supply is adjusted to +5.0 volts. As the +5.0 volts increases towards the +7.0 volt overvoltage point the voltage on the gate of Q2 increases until it reaches +1,6 volts, at which time the thyristor is gated ON and the output line (P1 pin 34) is clamped to ground. Once the crowbar is tripped, the power supply must be deenergized and the cause of the overvoltage condition eliminated before the crowbar will be reset.

The regulator incorporates a remote sense capability for the positive output (pin 36) and the return (pin 38). These are jumpered at the power supply connector as follows: Pin 36 to 34 and pin 38 to 28 for the +5 INT regulator.

In the +5 EXT regulator positive sense line 1 pin 15 is terminated at the front panel test connector pin 54 and the return sense (pin 13) is connected to pin 56 of the front panel test connector.

4.13.5 PROGRAMMABLE POWER SUPPLY OPERATION. Each of the three programmable power supplies operates the same way as described below with reference to the +V power supply circuit shown on D2990. Transformer T1 develops approximately 26 volts RMS across terminals E16 and E17 which is rectified by full-wave bridge rectifier CR11 through CR14. The uA723 voltage regulator (AR4) provides a regulated output voltage into the base circuit of series pass transistor Q8 which provides the necessary source current for the output voltage. Programming resistors are provided (R34 through R41) to control the output voltage of the +V power supply over the range from +500 millivolts to +26.1 volts. The eight programming resistors are binary weighted (similar to a D/A ladder), resulting in 256 discrete programming steps. Resistor R41 is the least significant bit for the eight program input bits and provides a change in the output voltage of 100 millivolts. Correspondingly, resistor R34 is the MSB and when connected to ground will cause a 12,8 volt change in the power supply output voltage. Resistor R48 protects the base circuit of AR4 from excessive current and R49 limits the output current of the power supply to approximately 800 milliamperes,

The operation of the -V power supply is identical to the +V power supply operation, The ±V power supply (AR5 also operates in the same manner with the following exceptions. Transistor Q9 sources approximately 800 milliamperes and the additional circuit consisting of Q10 and Q11 provide a negative output capability which sinks approximately 800 milliamperes. Because of the current sinking capability, the minimum voltage to which the ±V supply can be programmable is 1.0V.

SECTION V
MAINTENANCE

5-1 INTRODUCTION.

This section provides the maintenance technician with routine maintenance, preventive maintenance and troubleshooting information required to insure maximum Card Tester reliability and performance. Included are routine inspection procedures, mechanical and electrical adjustment procedures, fault isolation procedures and tables, and card reader repair information.

5-2 PREVENTIVE MAINTENANCE.

5-2.1 GENERAL GLEANING AND INSPECTION. Thoroughly inspect and clean the Card Tester at regular intervals depending on the operating environment. Remove dust and dirt from the chassis with a soft bristled brush used in conjunction with a suction hose. Remove hardened deposits and grease with a lint-free cloth moistened with an approved cleaning agent.

To ensure reliable operation of the card reader, the spring contacts and printed circuit board must be kept free of dirt, grease and other foreign matter. Several methods of cleaning are acceptable without removing the spring and block assembly when environmental conditions are relatively dust-free. Under extreme conditions it may be necessary to remove the spring and block assembly to remove excessive contamination, refer to paragraph 5-2.2 for detailed instructions for cleaning operations requiring removal of the spring and block assembly. Clean -the reader as follows:

a. Remove the Card Tester from the portable cabinet (bench mount model) .
b. Clean all surfaces of the card reader with a lint-free cloth or

or camel hair brush and Isopropyl Alcohol, or other approved cleaning agent equivalent.

c. Using dry-filtered air or a dry-pumped nitrogen supply of 15 PSI maximum pressure, blow through the front of the card reader receiver slot to remove dust particles from the contact springs and printed circuit board.

d. If a dry-filtered nitrogen or air supply is not available, the spring contacts and printed circuit board may be sufficiently cleaned by using a charged-surface mylar card. Place the card reader handle to the full CCW position (open) and insert the charged-surface card (with the charged side facing up) into the receiver slot, then remove the card, wipe it clean and insert in the receiver slot with the charged surface down.

CAUTION

DO NOT rotate the card reader handle (closing the receiver) CW with the charged-surface mylar card in place.

d. Reinstall the Card Tester chassis in the portable cabinet and perform a complete functional Self Test on the Card Tester according to paragraph 3-3.

5-2.2 CARD READER OVERHAUL PROCEDURES. Under normal operating conditions the card reader should require no more than occasional cleaning and inspection to maintain the unit in continuous and reliable operating order. The following overhaul procedure should be performed only when it is deemed necessary, after the general cleaning and inspection procedures fail to correct card reader malfunctions. This procedure requires that extensive disassembly of the Card Tester wiring harnesses and card reader unit be taken. To perform the overhaul procedure the maintenance technician must remove the card reader from the Card Tester chassis, as described in paragraph 5-2.2.1 below.

5-2.2.1 Card Reader Removal. Perform the following procedure, to the extent necessary, to gain access to the interior of the card reader prior to

performing cleaning and maintenance operations.

a. Disconnect the AC power cord from the wall receptical.

b. Remove the Card Tester chassis from the portable cabinet, if provided, by removing the four screws in the front panel. After removing the four screws, insure that the AC power cord does not become entangled in the cabinet and slide the chassis forward, out the front of the cabinet.

c. Remove the card reader mechanism from the Card Tester front panel and slide it out of the chassis by disconnecting the wiring into the card reader (both unplugging and unsoldering the necessary wiring), removing the receiver handle and removing the four 10-32 nuts from the front panel. Care should be taken when removing the wiring from the card reader matrix such as marking and identifying all wiring removed, carefully unsolder bus bar wiring and ensure that loose solder does not splash into the matrix, and due to the close location of the wiring harnesses to the card reader, ensure that the wiring is not damaged as the unit is slid away from the chassis. Return all mounting hardware to the studs or holes from which it is removed to avoid misplacing the hardware while performing maintenance procedures.

5-2.2.2 Overhaul Inspection. Perform the overhaul inspection in accordance with the following procedure:

a. Inspect all components and parts for security and/or damage. Replace damage parts in accordance with paragraph 5-5.2.2 if necessary.

b. Inspect all wiring for loose connections and frayed, cracked or worn insulation. Repair and/or replace wiring found to be defective.

c. Inspect card reader for cleanliness. Clean card reader as prescribed in paragraph 5-2.1.

Note

To properly clean the Printed Circuit board and spring block assembly, the assembly must be disassembled as described in paragraph 5-5.2.1.

d. Visually inspect the Contact Springs and Block Assembly for alignment and bent or broken Contact Springs. Repair or replace complete assembly as described in paragraph 5-5.2. Refer to section VI of parts identification and ordering information.

e. Thoroughly inspect the Printed Circuit board assembly for evidence of arcing or excessively worn spots. If damage is found, replace the Printed Circuit board as described in paragraph 5-5.2.

f. Inspect card reader for proper adjustments as delineated in paragraph 5-3.2.

g. Inspect eccentrics for security to shaft. Tighten set screws if necessary. See paragraph 5-3.2.4.

h. Inspect shaft for freedom of rotation. Replace needle bearing, if necessary, in accordance with paragraph 5-3.2.3.

i. Clean the internal workings of the card reader as delineated in paragraph 5-2.2.3.

5-2.2.3 Overhaul Cleaning. Perform overhaul cleaning of the card reader using Isopropyl Alcohol, or an approved equal, on a lint-free cloth and/or small brush in accordance with the following procedure.

a. Generally clean the frame and operation mechanism to remove any evidence of contamination.

CAUTION

The contact springs are critically adjusted at the factory for registration and contact closure. Take the necessary precautions to avoid bending or breaking the contact springs when performing b below.

b. With the Spring and Block Assembly removed, thoroughly clean the contact springs to remove any foreign matter such as dust particles, oil

film and/or corrosion.

c. With the Spring and Block Assembly removed, thoroughly clean the Printed Circuit Board to remove contamination such as dust, oil film, and/or corrosion.

d. Reinstall the card reader in the Card Tester as delineated in paragraph 5-2.2.4.

5-2.2.4 Overhaul Reassembly. Perform the following steps to reinstall the card reader in the Card Tester.

a. Slide the card reader into the proper location on the Card Tester front panel and fasten with the four 10-32 nuts removed during disassembly.

b. Connect the necessary wiring according to the identifying tags attached during disassembly. Ensure that solder is not splashed into. the card reader matrix or Contact Spring assembly during the soldering process.

c. Tighten all mounting hardware, insert Ty-Wraps where necessary, and complete installation of card reader in Card Tester.

d. Perform the Spring and Block assembly adjustment procedure given in paragraph 5-3.2.6.

e. Perform the Contact Springs Deflection Adjustment in accordance with paragraph 5-3.2.4.

f. Verify the proper operation of the Card Reader by performing the Self Test procedures delineated in paragraph 3-3. Once Self Test operations are completed with satisfactory results, slide the Card Tester chassis back into the portable cabinet, if applicable, and tighten the four screws holding the chassis into the front panel. If any malfunctions occur during Self Test, refer to the Card Tester troubleshooting procedures and tables in paragraph 5-4.

5-3. ADJUSTMENTS.

Procedures are provided in paragraph 5-3.1 for adjusting the power supplies. All power supply adjustments have been precisely set at the factory and should require no further adjustment unless repair work is performed on the internal power supply circuits. Several card reader adjustments are required

if the card reader malfunctions and/or requires extensive maintenance. These adjustment procedures are delineated in paragraph 5-3.2.

5-3.1 POWER SUPPLY ADJUSTMENT PROCEDURES.

5-3.1.1 +5 Volt External Power Supply Adjustment Procedures. The +5 volt external power supply provides an adjustable power supply voltage which is wired to pin 54 of the CARD IN TEST connector and can be connected to any of the 54 programmable pins on the test connector. The +5 volt external power supply is adjusted in accordance with the following steps:

a. Energize the Card Tester by inserting a program card into the card reader receiver, see paragraph 3-4.

b. Monitor the +5 volt external power supply output voltage at TP 22 (+5 EXT) on the front panel with a DC voltmeter. Negative lead from meter connects to GRD test point.

c. Adjust potentiometer R12 (+5 EXT), located through the hole in the rear of the chassis, to the desired output voltage.

5-3.1.2 +5 Volt Internal Power Supply Adjustment Procedure. The +5 volt internal power supply is factory adjusted and should not be adjusted unless repair work has been performed in the associated power supply circuitry. In this case, the +5 volt internal power supply output voltage should be adjusted according to the following procedures:

a. Energize the Card Tester by inserting a program card into the card !reader receiver, see paragraph 3-4.

b. Monitor the +5 volt internal power supply output voltage at TP 23 (+5 INT) on the front panel. Place the positive lead of a DC voltmeter in TP23 and the negative lead into the GRD test point.

CAUTION

In the following step, DO NOT exceed +5.25 volts while adjusting the internal +5 volt power supply output.

Damage to the internal Card Tester can result if the +5 volt internal power supply is adjusted beyond +5.25 volts.

c. Adjust potentiometer R2 (+5 INT) for a meter reading of +5.0 volts DC. Rotating the potentiometer CW increases the output voltage.

5-3.1.3 Programmable Power Supply Adjustment Procedures. Each of the three programmable power supplies, +V, -V and +V, is adjusted at the factory and require no further adjustment unless, circuit repair has been performed in the associated power supply internal circuits. All three power supplies operate in the same manner and therefore, are adjusted in the same manner. Both an OFFSET and GAIN adjustment are provided for each power supply, located at the rear of the chassis and labeled according to the respective power supply. Test points, used for monitoring the power supply outputs during adjustment procedures, are located for the individual power supplies on the front panel. The following steps provide the necessary power supply adjustment sequence for each of the programmable power supplies:

a. Connect a digital voltemeter (or equivalent) to the appropriate power supply output test point on the front panel.
b. Insert "power supply test #1" program card (see figure 5-1) into the Card Tester.

Note

The +V power supply is programmed to output positive voltages for all adjustment procedures related to this power supply.

c. Adjust the power supply output being monitored to 26.1 volts DC using the corresponding power supply GAIN adjustment as listed below:

1. -V GAIN (R16) adjusts -V power supply output.

2. +V GAIN (R43) adjusts +V power supply output.
3. +V GAIN (R61) adjusts ±V power supply output.

d. Remove power supply test #1 program card and insert power supply test #8 program card into the Card Tester.

e. Adjust the power supply output being monitored to 1.0 volt DC using the corresponding power supply OFFSET adjustment as listed below:

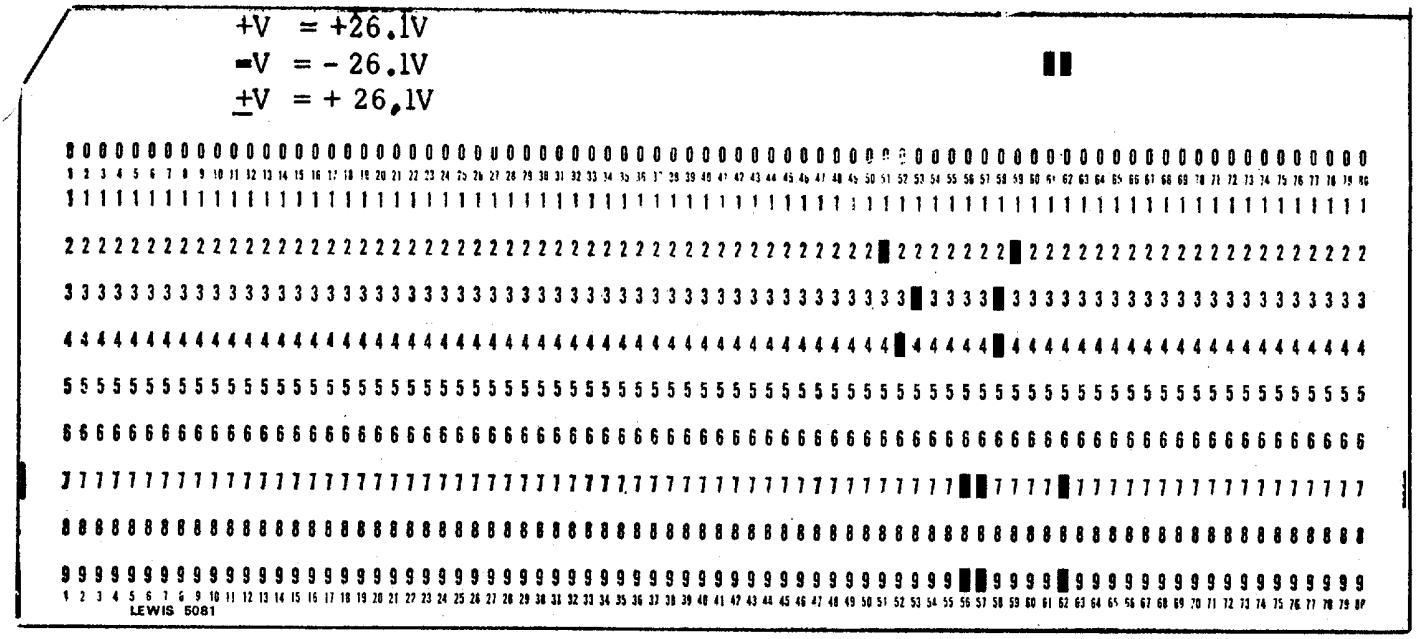
1. -V OFFSET (R19) adjusts the -V power supply output.
2. +V OFFSET (R46) adjusts the +V power supply output.
3. ±V OFFSET (R64) adjusts the ±V power supply output.

f. Repeat b through e above until both the output voltages readings are obtained without further adjustment.

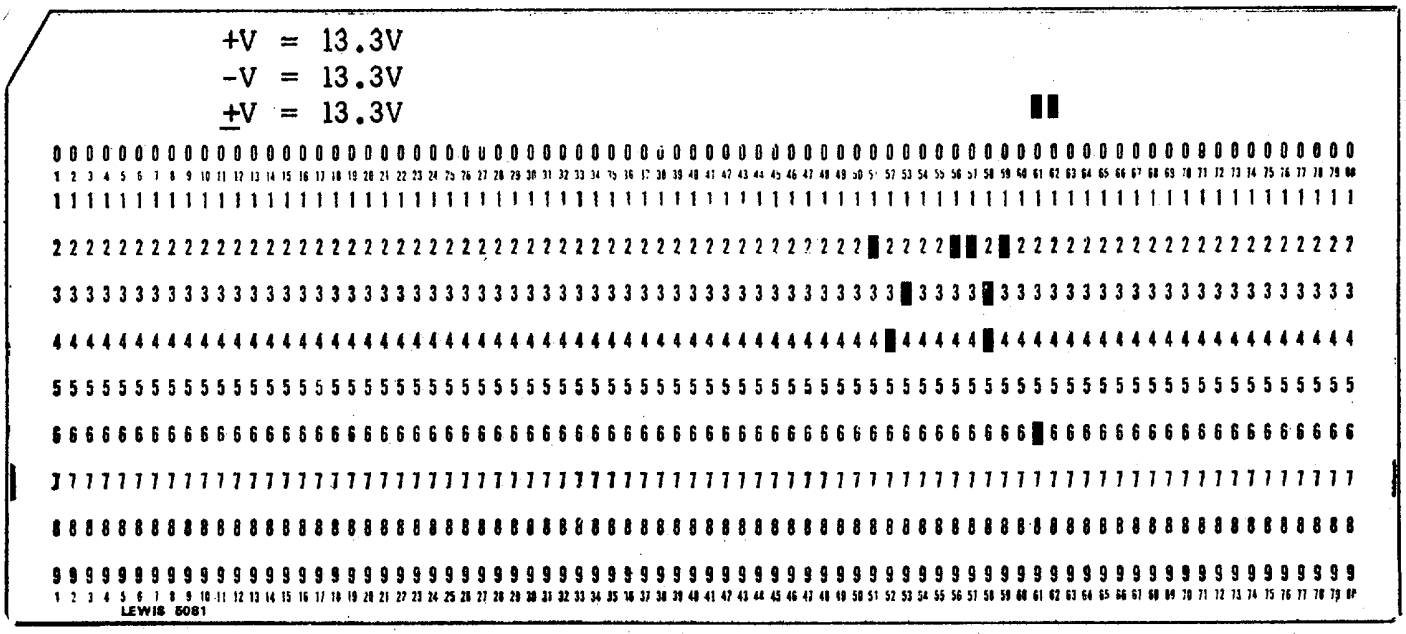
g. Remove the last power supply test program card in the Card Reader and insert the additional power supply program cards (as shown in figure 5-1) to verify the power supply tracking linearity. The corresponding output voltage for each power supply is written on the test program cards illustrated in figure 5-1.

CAUTION

If repair is performed on the power supply and assembly A1 is loosened (or removed) DO NOT exceed a torque of 8 inch pounds on the eight screws used to secure the printed circuit board into the power supply.

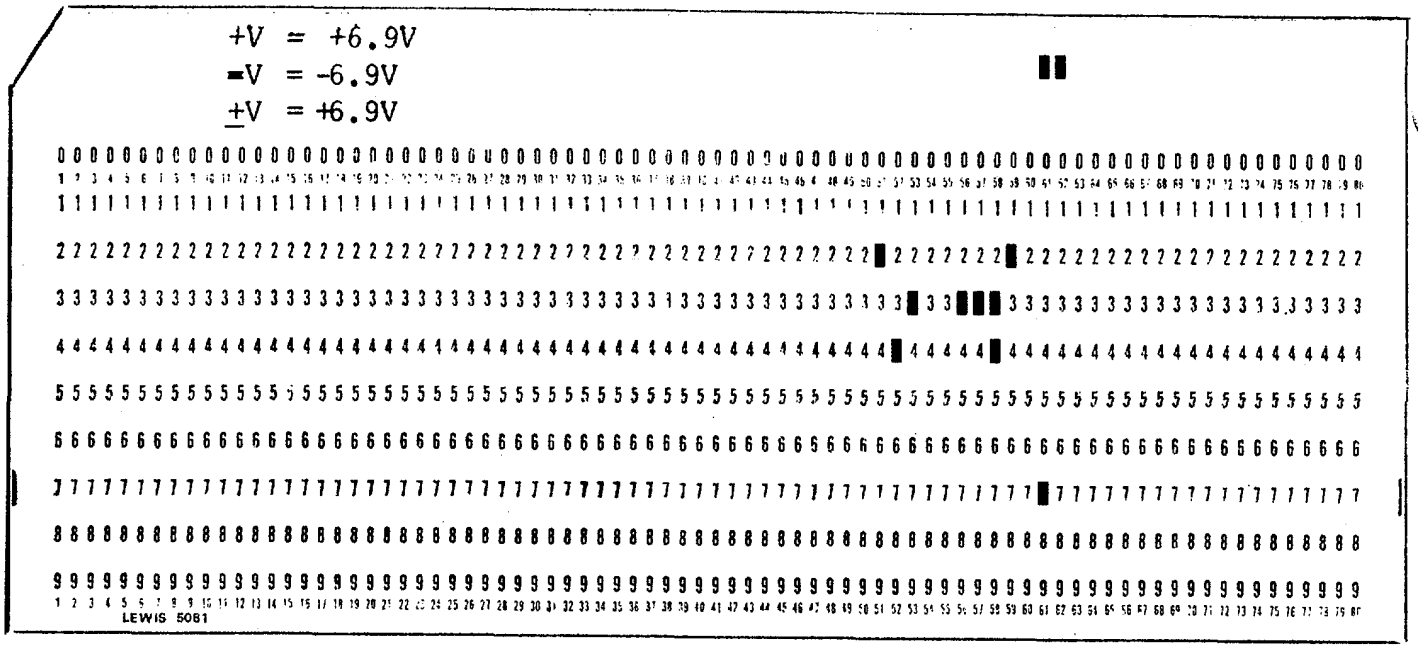


(A) P.S. Test Card #1

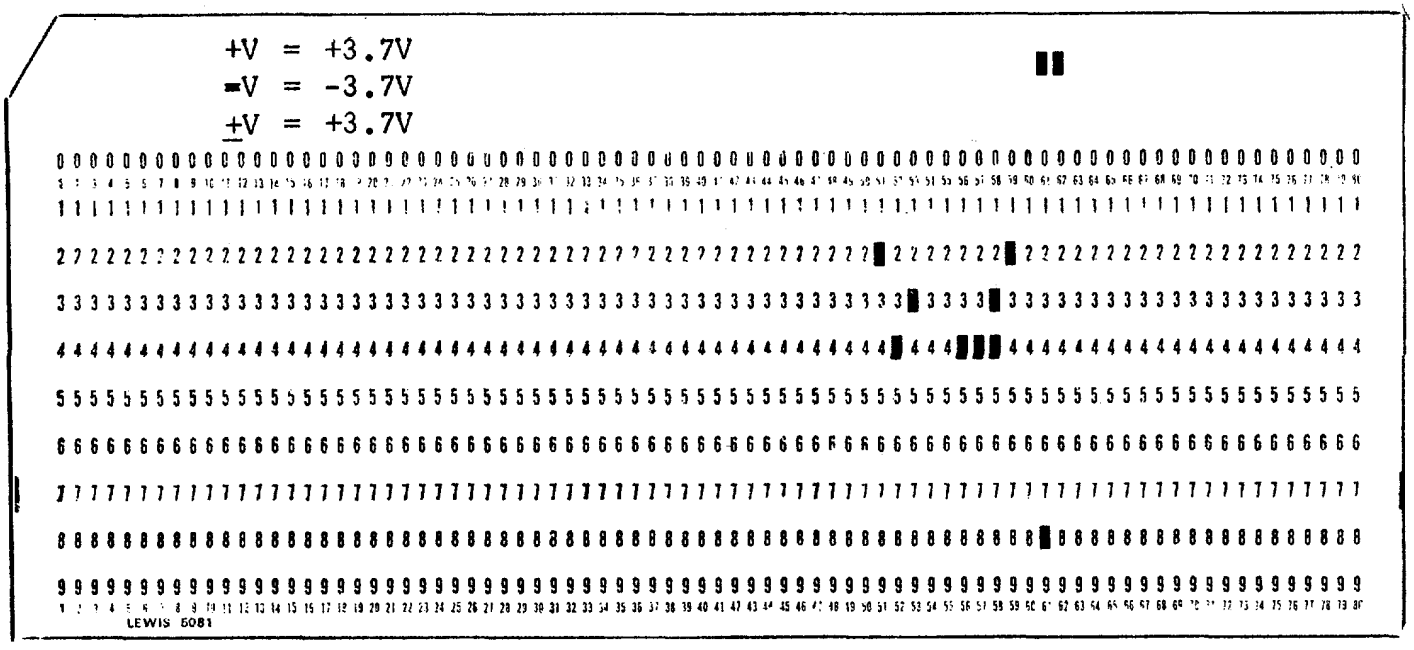


(B) P.S. Test Card #2

Figure 5-1. Power Supply Test Programs (sheet 1 of 4)

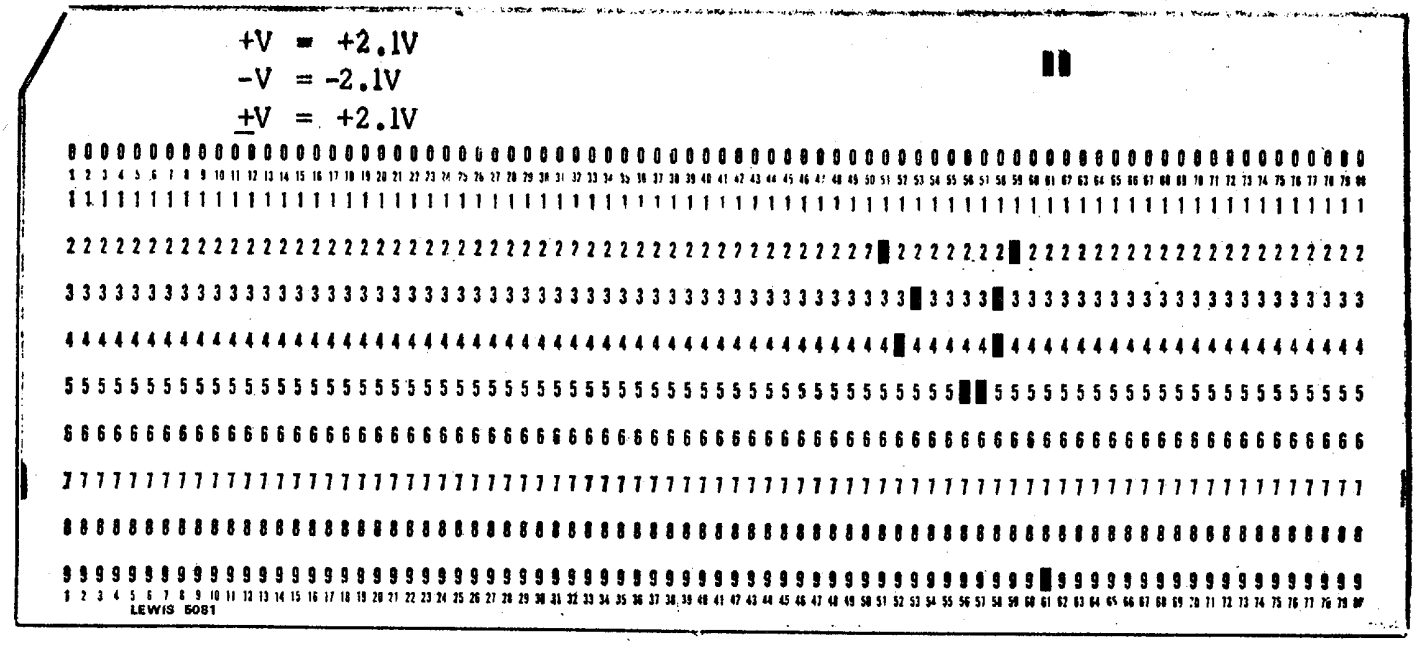


(C) P.S. Test Card #3

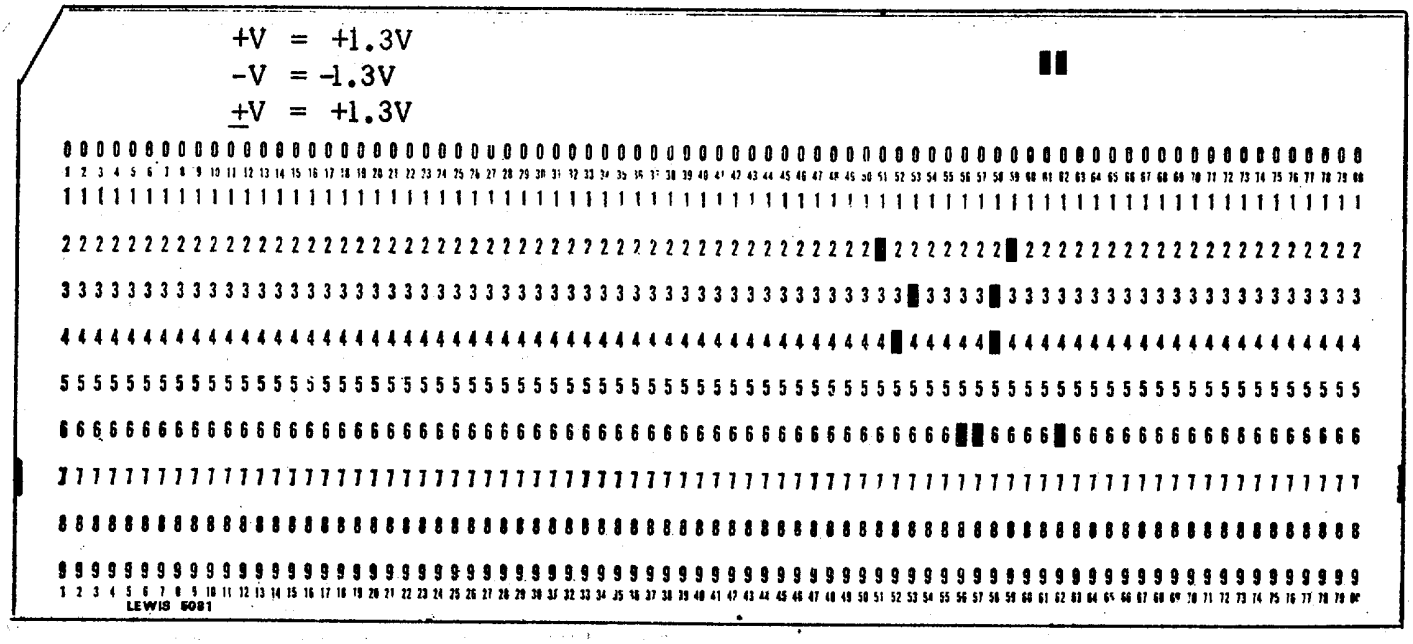


(D) P.S. Test Card #4

Figure 5-1. Power Supply Test Programs (sheet 2 of 4)

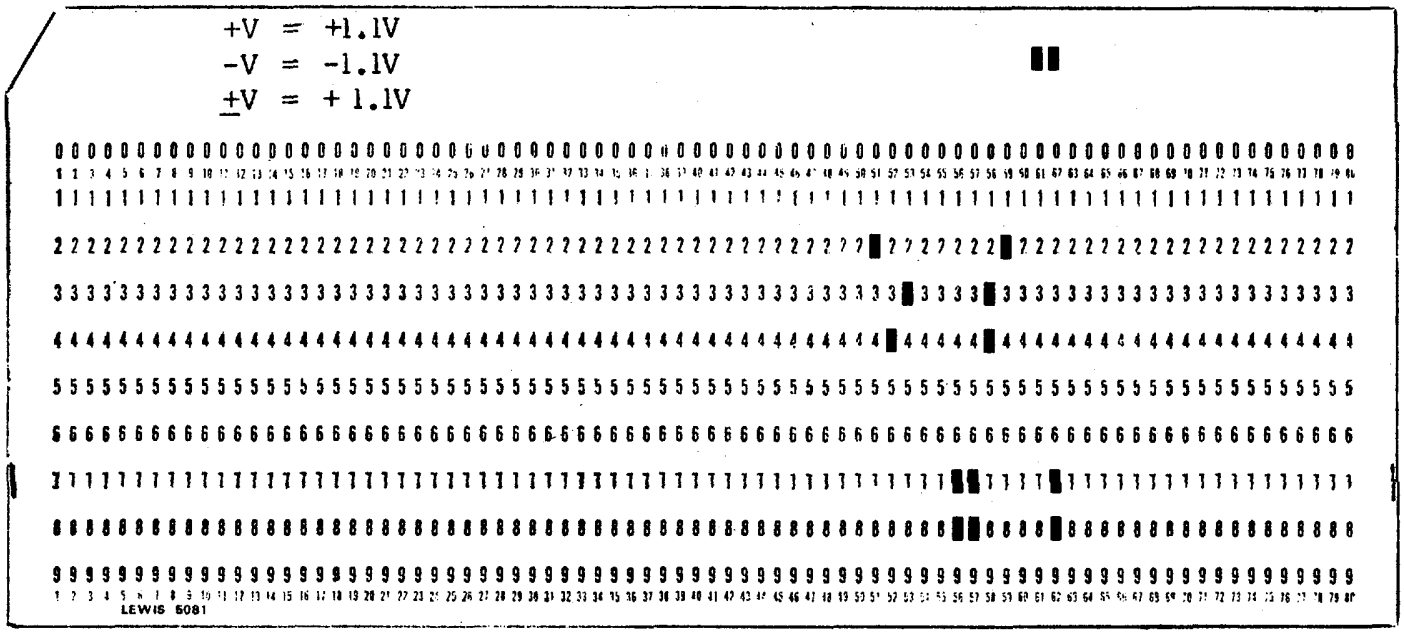


(E) P.S. Test Card #5

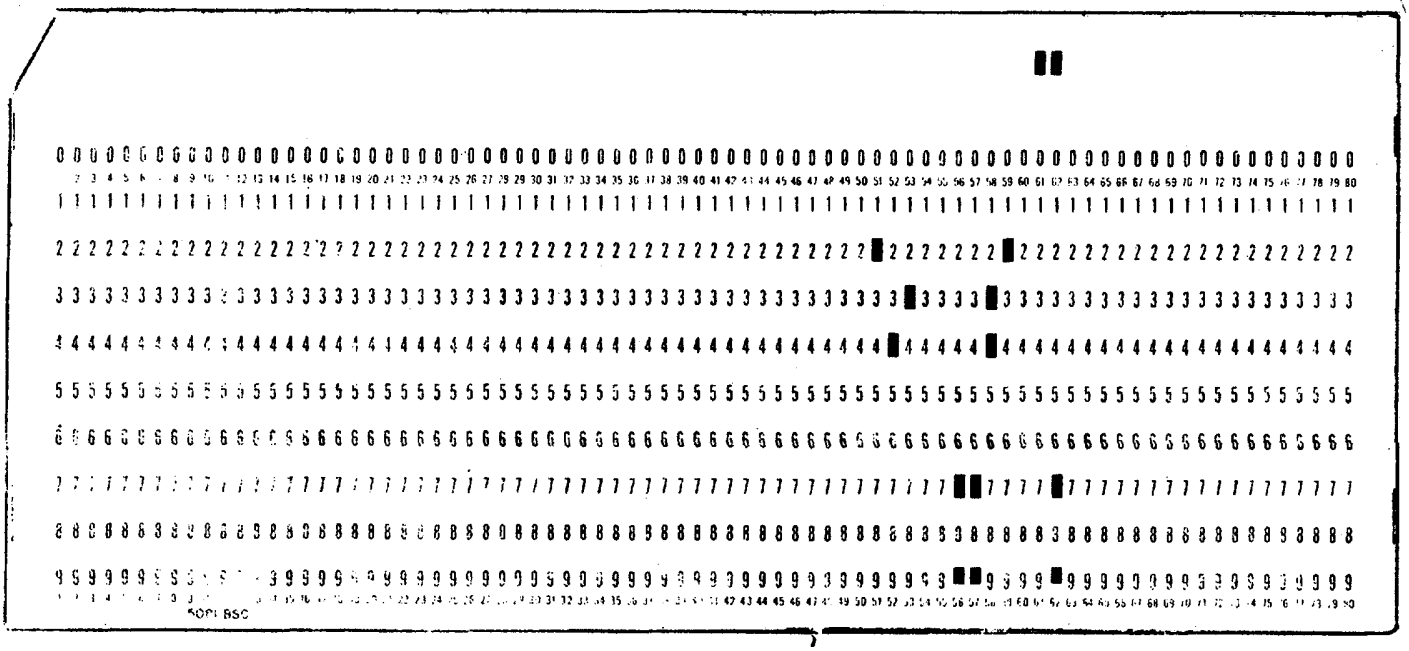


(F) P.S. Test Card #6.

Figure 5-1. Power Supply Test Programs (sheet 3 of 4)



(G) P.S. Test Card #7



(H) P.S. Test Card #8

Figure 5-1. Power Supply Test Programs (sheet 4 of 4)

5-3.2 CARD READER ADJUSTMENTS

5-3.2.1 General. The following paragraphs give the procedures for checking and/or making adjustments as may be required by Periodic Maintenance, Troubleshooting, Repair and/or Replacement as described herein.

5-3.2.2 Card Insertion Switch Adjustment. (See Figure 5-2)

a. Connect leads of a standard ohmmeter to the (common) and NO (normally open) posts on the Card Insertion Switch.

b. Insert a Card into the Unit until it hits against the Card Stop. The Switch MUST close .005 to .015 inch before reaching the Card Stop.

c. If Switch does not close within the above tolerance, loosen the two mounting Screws and move Switch forward or back until the correct setting is obtained.

d. Retighten mounting Screws, then repeat b above.

e. Remove Card and ohmmeter from Unit.

5-3.2.3 Eccentric/Shaft Adjustment. (See Figure 5-3)

a Us astandard feeler gauge to check end play of Shaft. End play MUST BE .015-inch maximum between nylon Washer and the Frame.

b. If end play is not within tolerance loosen set screw in front or rear Eccentric and slide in the direction required to obtain clearance within limits.

Note

Pin through back end of Shaft MUST align with Card Read Switch actuator. This will determine which Eccentric should be adjusted.

c. Retighten set screw in Eccentric, then recheck end play as described in a above to assure clearance is within tolerance.

5-3.2.4 Contact Springs Deflection Adjustment. (See Figure 5-4)

a. Check Contact Springs deflection by fully closing the Unit.

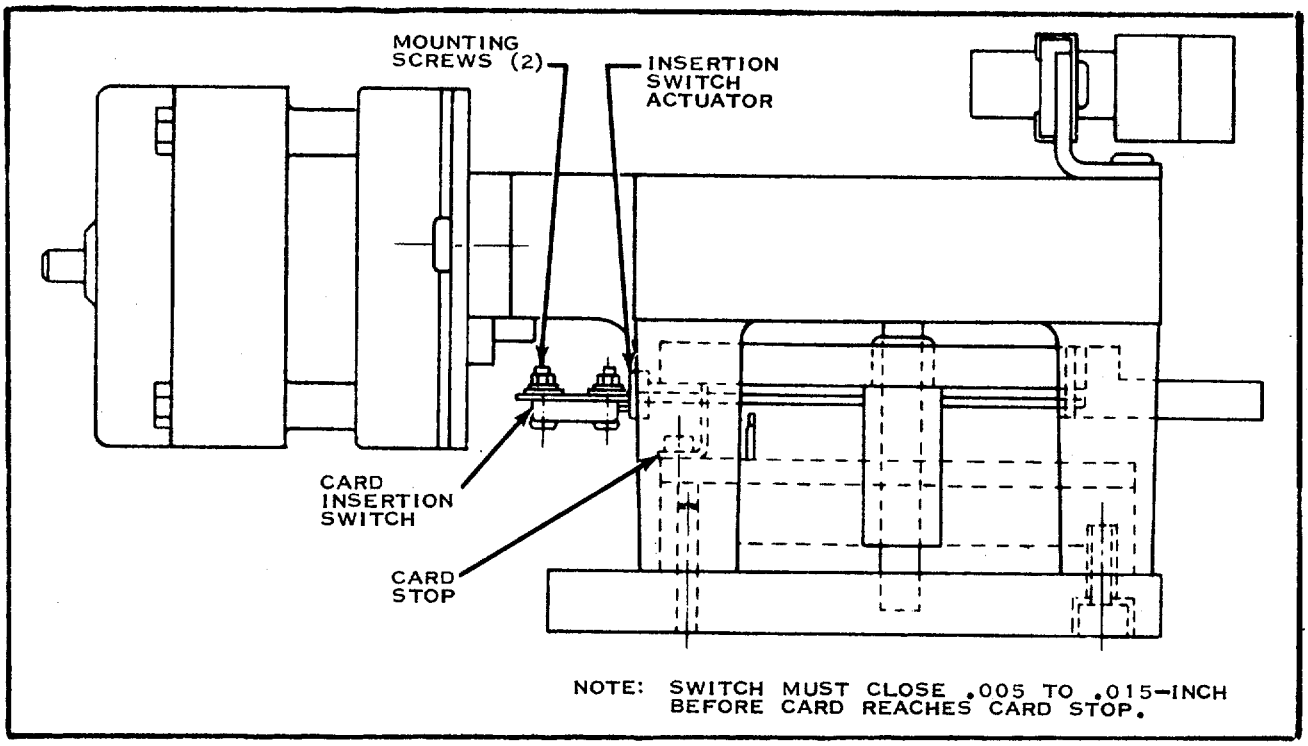


Figure 5-2. Card Insertion Switch Adjustment

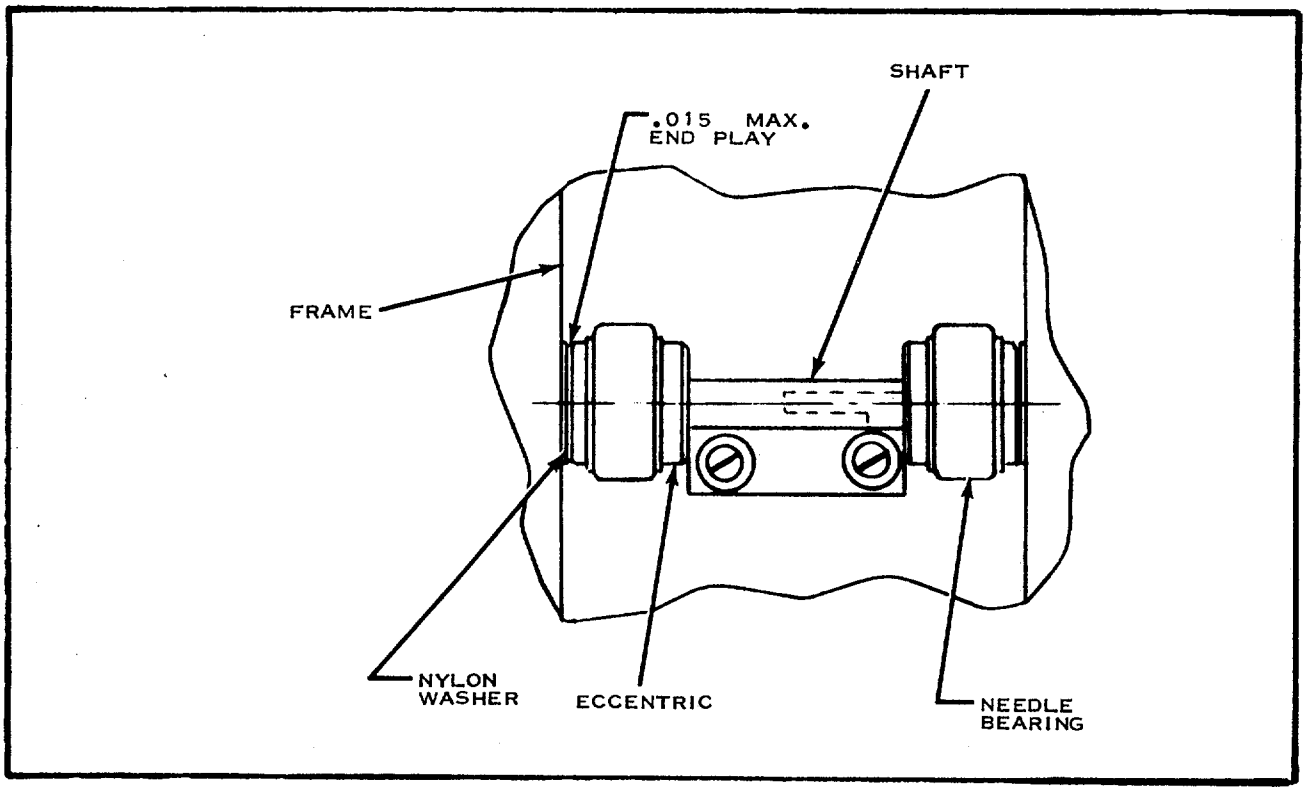


Figure 5-3. Typical Eccentric/Shaft Adjustment

b. With Unit fully closed, attach a dial indicator to the Frame (94) over the Entrance Lip (72), then position the indicator plunger against the top of the Lip and adjust to zero.

c. Reopen Unit manually, then partially close Unit until Printed Circuit Board (74) contacts the Contact Springs. Indicator MUST read .020 ± .010 inch before zero.

d. If reading is not within tolerance, reopen the Unit and perform e, f, and g below.

e. Remove Base or Bars, with Spring and Block Assembly (50) attached, by removing four Screws from legs of Frame. Refer to Figure 6-2.

f. Add or subtract Shims as necessary to bring Contact Springs deflection within tolerance.

Note

Make certain the same thickness of Shims are added or subtracted to the four Frame legs. Under certain circumstances, it may be necessary to make contact location adjustments by physically deforming the Contact Springs. If this is necessary, exercise extreme care in performing the operation to prevent permanent damage to the Contact Springs.

g. Replace Base or Bars with four Screws, then repeat above Steps to assure setting is correct.

h. Reopen Unit and remove dial indicator.

5-3 2.5 Card Stop Adjustment. (See Figure 6-2)

CAUTION

DO NOT attempt adjustment of the Card Stop (46) unless it was necessary to replace it because of damage.

a. Remove Spring and Block Assembly (50) in accordance with paragraph 5-5.2.1.

b. Select a fully punched Card that has been checked for accuracy on a Card Gauge.

c. Slightly loosen the two Screws (45), then slide Card Stop toward the rear.

d. Position Card over Contact Springs of Spring and Block Assembly, centering punched holes longitudinally with the Contact Springs.

e. Holding Card in proper alignment, slide Card Stop against edge of Card until both ears contact evenly. Retighten Screws and recheck setting. Repeat procedure if necessary.

f. Replace Spring and Block Assembly in accordance with 5-5.2.3, then check adjustment as described in paragraph 5-3.2.6. Adjust if necessary.

g. Check adjustment of Card Insertion Switch as described in Paragraph 5-3.2.2. Adjust if necessary.

5-3.2.6 Spring and Block Assembly Adjustment. (See Figure 6-2)

Note

The following procedure must be performed each time the Spring and Block Assembly (50) is removed from the Unit.

a. With the Unit fully assembled, partially close Unit manually while visually observing Contact Spring alignment with holes in Card Guide Assembly (73). Contact Springs MUST enter hole centers longitudinally without touching. If not centered perform the following Steps.

b. Slightly loosen four Screws (38) securing Spring and Block

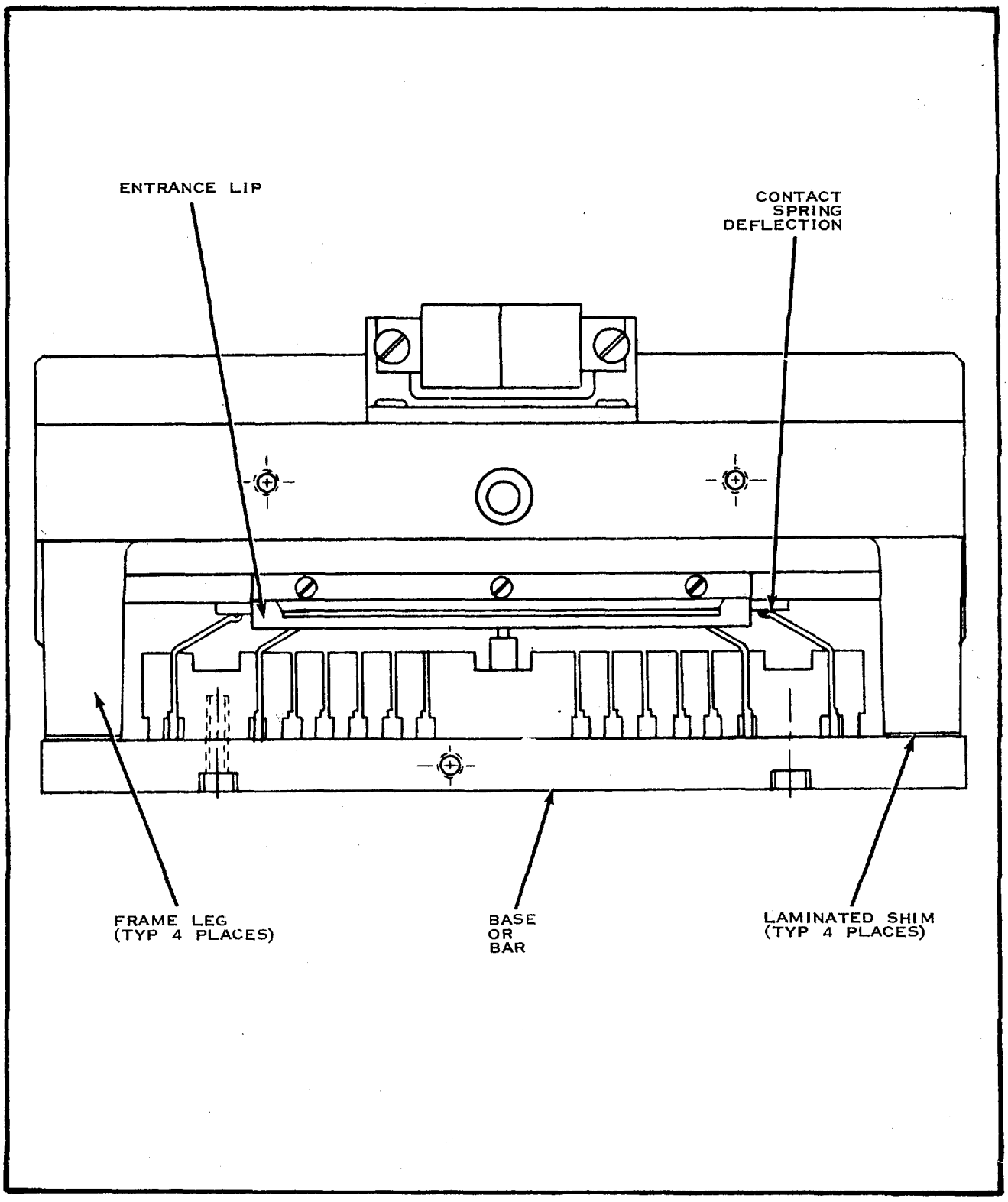


Figure 5-4. Contact Springs Deflection Adjustment

Assembly to Machined Base (40) or Mounting Bars (41).

c. Loosen four Screws (34) securing Machined Base or Mounting Bars to Frame (94) to provide .030-inch gap.

d. Manually close Unit while making certain Contact Springs are approximately centered in holes of Card Guide Assembly. Center the Contact Springs in the holes by sliding Spring and Block Assembly in the desired direction. Retighten all Screw.

e. Recheck setting by opening and closing Unit several times. Contact Springs MUST enter without scraping. If necessary, repeat Steps (a.) through (e.) until proper adjustment is obtained.

5-4. TROUBLESHOOTING.

Troubleshooting procedures for the Card Tester and internal card reader are provided in the following paragraphs to aid the maintenance technician in isolating probable malfunctions. These instructions, executed with normal troubleshooting techniques, should isolate the defective circuit, component and/or mechanical malfunction to a replaceable part, or in the case of the card reader, determine the cleaning or applicable adjustment procedure to correct the malfunction. Care should be exercised when analyzing suspected Card Tester troubles to ensure that the condition is not caused by incorrect switch settings, improper program card, incorrect insertion of program card into card reader receiver slot or conditions caused from the external card-under-test. In addition, the maintenance technician must be careful to isolate the symptoms to the most likely cause, avoiding possible disassembly of the card reader (which should be executed only as a last resort) for malfunctions caused by the internal Card Tester circuits associated with the card readers.

5-4.1 CARD TESTER FAULT ISOLATION. Fault isolation techniques for the Card Tester include, for the most part, execution of the automatic Self Test and Self Test programs A and B. These three programs provide ample testing to isolate most probable malfunctions which are likely to occur in the Card Tester over a long period of operation. The troubleshooting charts provided in table 5-1

are directly related to the Self Test procedures delineated in paragraph 3-3. Localization of malfunctions beyond the limits of the information provided in table 5-1 are implemented through generally accepted troubleshooting techniques. Isolation of printed circuit card malfunctions is implemented by testing the suspected defective printed circuit card in a second Card Tester. Test programs are provided in section IX of this manual to aid the technician in determining faulty circuits within the internal card themselves. Refer to section IV for detailed descriptions of functional circuit theory of operation and section VIII for printed circuit card technical characteristics, parts information, and detailed schematic/logic diagrams.

5-4.2 CARD READER TROUBLESHOOTING. In many cases, problems with the card reader are quite obvious because, the nature of the malfunction isolates the source of the problem to a mechanical part or operation. Malfunctions associated with reading the IBM card, on the other hand, are a bit more difficult to determine the cause. Before attempting to disassemble the card reader for troubleshooting a particular problem, ensure that the cause of the trouble originates in the card reader and not in the associated circuits comprising the Card Tester. The card reader is fully adjusted at the factory for mechanical registration and precisely calibrated for reliable operation for many years. If maintenance is required on the card reader, take the necessary precautions not to disturb areas other than those directly associated with the malfunction. Table 5-2 lists typical symptoms, their probable cause and the corrective action necessary to remedy the cause.

Table 5-1 Card Tester Fault Isolation

PAR/STEP	SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION (DRAWING REFERENCE)
3-3.1 (a.)	Card reader does not accept program card	See Table 5-2	See Table 5-2
3-3.1 (b.)	POWER ON indicator remains OFF	AC power cord not plugged in	Plug AC power cord in 115 VAC power source.
		AC input fuse (FI) blown	Replace F1. (D2990)
		Lamp fuse (F2) blown	Replace F2. (D2990)
		POWER ON indicator burned out.	Replace POWER ON switch/indicator lamp, See section VI.
3-3.1 (c.)	GO indicator does not light and/or NO-GO indicator remains lit.	Timing Oscillator defective.	Replace PC card 2A. (D3000)
		Self Test flip-flop D1 defective	Replace PC card 1A. (D3005)
		Self Test Flip-flop D2 defective	Replace PC card IA. (D3005)
		GO indicator burned out	Replace GO indicator lamp. See section VI (D3008)
	INPUT FAULT indicator lights	Programmable Driver/ receiver loop faulty	Determine which row is malfunctioning troubleshoot according to the following steps.

Table 5-1 Card Tester Fault Isolation (Cont'd)

PAR/STEP	SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION (DRAWING REFERENCE)
			Temporarily insert Self Test Program "A" card into the card reader (operates the test signal generator at a faster rate) and observe Test Signals +CO through +S2 (output pins 1 through 10 respectively). Missing output test signal identifies corresponding programmable driver/receiver loop (ROW) which is faulty. The following procedure lists the steps necessary to isolate the malfunctioning circuit within the ROW loop, with respect to row 1. All other rows (row 2 through 10) are tested in a similar manner. Using an oscilloscope, check level at 7A-TP7 (D3003). High level indicates another ROW is at fault, check all flip-flop outputs for a low level. Low level at 7A-TP7 indicates ROW 1 is faulty. (D3003) Check 4A-TP5 for test signal +C0 (D3004) while pressing the TEST NO-GO (Reset) switch/indicator. If no signal on 4A-TP5, check for test signal +C0 on front panel test point. If no signal on front panel test point, replace PC card 1A. If +CO is

Table 5-1 Card Tester Fault Isolation (Cont'd)

PAR/STEP	SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION (DRAWING REFERENCE)
			present on front panel test point replace PC card 4A. If test signal +CO is present on 4A TP5 (D3004) while pressing the reset switch, observe 6A TP 11 (D3003) for +CO test signal. If +CO is not present on 6A-TPll replace receiver card 6A or troubleshoot stage AR2 of the card. If +CO is observed on 6A-TP11 troubleshoot stages Al and El of fault detector card 7A (D3003). Once troubleshooting procedures are completed, remove Self Test Program "A" from the reader and insert Automatic Self Test program card into card reader and continue with paragraph 3-3.1 step (d.)
3-3.1 (d.)	GO indicator remains lit while NO-GO is pressed.	Counter packs E,F,K, J, or M on card IA defective. Flip-flop H2 on card 3A defective.-	Check PC card IA TP 5 for 122 Hz square wave. If no output on TP 5, check the following points (D3000): IA TP7 - 976 Hz 1A TP9 - 15.6 KHz 1A TP11 - 250 KHz 2A TP23 - 4 MHz If 1A TP 5 output signal present, check 1A TP23 for 7.6 Hz square wave. (If no out-put, replace IC pack 1A-Ml) Connect scope probe to 3A TP10 (D3002) and momentarily press the NO-GO indicator,

Table 5-1 Card Tester Fault Isolation (Cont'd)

PAR/STEP	SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION (DRAWING REFERENCE)
			observe that TP10 remains low for at least 1 millisecond after the switch is released. If not, replace IC pack 3A-H2. If delay Reset output is okay, 3A-H2, replace Self Test flip-flop 1A-D1.
	NO-GO indicator does no light	Make the same checks as for the GO indicator above. If above checks are good, check Self Test flip-flop 1A-D2.	Replace IC pack 1A-D2 if defective.
3-3.1 (e.)	NO-GO indicator ON and GO indicator OFF.	+B7 test signal at a low, level or Test Rate select - gates inoperative	Connect scope probe to PC card 1A, TP3 and observe 122 Hz square wave. If incorrect output is observed, replace IC pack 1A-A1, if defective. (D3000) **Note** For the following checks it is recommended - that Self Test Program card "A" be temporarily inserted in the card tester to operate the Test Signal generator at a faster rate. Connect scope probe to test signal +B7 (test point located on front panel). If no output is observed, move the probe one test point at a time towards +B0 until

Table 5-1 Card Tester Fault Isolation (Cont'd)

PAR/STEP	SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION (DRAWING REFERENCE)
			a square wave output is present. Replace the IC pack associated with the last bad output.
	NO-GO indicator remains OFF and GO indicator remains ON.	Test Signal +B7 is at a high level, make the same checks as delineated for the malfunction above.	Same as above.
3-3.1 (f.)	NO-GO indicator remains ON and/or GO indicator is OFF.	Test signal +C5 is incorrect ("C" Signal Generator is malfunctioning)	Temporarily insert Self Test Program "A" card into the card reader (operates the Test Signal generator at a faster rate) and observe Test Signals -C5 through +C0. If found to be defective, replace PC card2A or further isolate trouble in "C" Clock Generator (D3001).
		Signal +FR START is incorrect	Connect scope probe to the SYNC test point on the front panel and observe +FR START pulse at beginning of frame. If incorrect, determine source of malfunction from Frame Start Decoder in D3001.
3-3.1 (g.)	NONE		
3-3.1 (h.)	NONE		
3-3.1 (i.)	GO indicator remains OFF.	Programmable flip-flop 3A-B2 does not function properly.	Refer to paragraph 3-3.2 (Self Test Program A) and select output pin 9 to verify the proper operation of

Table 5-1 Card Tester Fault Isolation (Cont'd)

PAR/STEP	SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION (DRAWING REFERENCE)
			programmable flip-flop 3A-B2. Replace IC pack 3A-B2 if defective (D3005).
	NO-GO indicator remains ON	WAVEFORM TEST switch B is in wrong position	Set switch B to go position 7.
		Bit Counter is defective	Connect scope probe to 3A TP21 and observe 60 Hz square wave. If 60 Hz is not present, replace IC pack 3A-E1, if defective. If 60 Hz is present on 3A-TP21, troubleshoot Bit Counter (D3002).
	GO indicator remains ON	WAVEFORM TEST switch A is in wrong position.	Set switch A to position 9.
		Edge detector or edge Counter does not operate correctly.	Connect scope probe to PC card 2A TP15 and observe low level output signal for each edge of test signal +B4o Pulse width If no output is present, troubleshoot Edge approximately 8.2 milliseconds. Compare circuit; if present, troubleshoot Edge Counter (D3002).
3-3.2 (a.)	Card does not release	See table 5-2, TROUBLE #4.	See Table 5-2.
3-3.2 (b.) through (e.).	GO indicator does not illuminate	Switch A positioned Incorrectly	Set switch A to the correct position.

Table 5-1 Card Tester Fault Isolation (Cont'd)

PAR/STEP	SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION (DRAWING REFERENCE)
		Switch B positioned incorrectly.	Set switch B to the correct position.
		IN/OUT SELECTOR switches positioned incorrectly.	Set IN/OUT SELECTOR switches to the correct position.
		Test Signal being tested is not correct	Troubleshoot Test Signal generator, programmable drivers and card reader matrix to determine malfunction (D3000, C3001, D3004).

Table 5-2 Card Reader Troubleshooting Table

TROUBLE	PROBABLE CAUSE	REMEDY
1. Unit will not receive Card	Unit not fully open.	Actuate Unit to the full open position.
	Card bent or torn.	Replace Card.
	Unit needs cleaning.	Clean Unit in accordance with paragraph 5-2.1.
	Entrance Lip damaged.	Replace Lip in accordance with paragraph 5-5.2.
	Card Guide Assembly damaged.	Replace Guide in accordance with paragraph 5-5.2.
	Card Reader Pin jammed.	Clean Unit in accordance with paragraph 5-2.1.
	Card Insertion Switch jammed.	Clean Unit in accordance with paragraph 5-2.1.
	Card Drive "O" Ring worn	Replace "O" Ring in accordance with paragraph 5-5.2 .
2. Unit will not close properly or freely.	Shaft binding.	Remove Shaft and replace parts as necessary in accordance with paragraph 5-5.2.
	Eccentrics not properly adjusted.	Adjust Eccentrics in accordance with paragraph 5-3.2.3
	Guide Bearing binding on Dowel Pins.	Clean and lubricate with one drop of oil or replace Bearings and Pins in accordance with paragraph 5-5.2.
	Slotted Pin connecting Shaft to Shaft. Collar broken.	Replace Pin(s) in accordance with paragraph 5-5.2.

Table 5-2 Card Reader Troubleshooting Table (Cont'd)

TROUBLE	PROBABLE CAUSE	REMEDY
2. Continued	Shaft Collar damaged or broken.	Replace Collar in accordance with paragraph 5-5.2.
3. Unit does not read	Card mispunched, bent, or. torn.	Replace Card
	Unit needs cleaning	Clean Unit in accordance with paragraph 5-2.1.
	Spring and Block Assembly not properly adjusted.	Adjust Assembly in accordance,- with paragraph 5-3.2.6
	Wiring to Spring and Block Assembly damaged or broken .	Repair and/or replace Wiring.
	Contact Spring(s) bent or broken.	Repair or replace Spring and Block Assembly in accordance with paragraph 5-5.
	Printed Circuit Board burnt or scored.	Replace Printed Circuit Board in accordance with paragraph 5-5.2
	External equipment defective	Check out external equipment.
4. Unit will not open and release Card at completion of read cycle.	Contact Spring bent or broken.	Repair or replace Spring and Block Assembly in accordance with paragraph 5-5.2.
	Card Guide Assembly damaged.	Replace Guide in accordance with paragraph5-5.2.
	Entrance Lip damaged .	Replace Lip in accordance with paragraph 5-5.2.

5-5 REPAIR AND REPLACEMENT.

5-5.1 CARD TESTER. Repair and replacement of parts within the Card Tester does not require special procedures other than standard shop practices normally used when repairing electronics equipments. All circuitry is contained on repairable printed circuit boards and all control devices are located on the front panel. For the bench mount model, the portable cabinet must be removed for access to the PC boards and rear of the front panel, which contains switch, test point, and CARD IN TEST wiring. Parts descriptions, part numbers and part identifying information are located in section VI. Component identification information for the printed circuit boards is located in section VIII. This information includes, component reference designators, parts lists, manufacturers names and addresses, and quantities required for individual printed circuit boards.

5-5.2 CARD READER. The following paragraphs describe the procedures necessary to disassemble, repair and/or replace worn or broken parts, and reassemble the card reader. Refer to the exploded views, fiqures6-l and 6-2, in section VI for part number identification, location and quantities required for the card reader. Refer to paragraph 5-4.2 for card reader troubleshooting procedures and table 5-2 for a tabular listing of probable cause and effect malfunctions.

5-5.2.1 Unit Disassembly (See Figure 6-1 and 6-2). Disassembly of the Unit, to the extent necessary to accomplish the repairs and/or replacement of components or parts shall be in the order of numerical sequence of Item Numbers. All Items for the card reader are covered.

During disassembly, the following procedure and precautions shall be observed.

a. Remove the card reader from the Card Tester by disconnecting and identifying all wiring (b below).

It is necessary to remove the Handle (9) by removing Pin (8) before the card reader is detached from the front panel.

b. When disconnecting wiring from the Unit, tag and identify

connectors for reinstallation purposes.

c. Unless damaged, the Card Stop (46) should not be removed.

CAUTION

DO NOT attempt to disassemble the Spring and Block Assembly (50).

5-5.2.2 Parts Inspection, Repair and/or Replacement (See Figure 6-2).

a. Inspect all parts for evidence of excessive wear, or other damage. Replace parts as required.

b. Inspect all wiring for breaks, frayed or damaged insulation, damaged or loose contacts,. and loose solder connections. Repair or replace wiring as deemed necessary to assure reliability.

c. Inspect Spring and Block Assembly (50) for bent or broken Contact Springs. If Contact Springs are bent beyond the possibility of straightening, or if broken, then the complete Assembly must be replaced.

d. Inspect Switch(es) for excessive play in switch Actuating Levers. Replace Switch(es) as necessary.

e. Inspect Extension Spring (52), Feed Roller Loading Spring (36), Compression Springs (42 and 47), as applicable, for distortion. Replace Spring(s) as necessary.

f. Inspect Printed Circuit Board (74) for evidence of damage by arcing or scoring. Replace Board if necessary.

g. Inspect Card Guide Assembly (73) and Entrance Lip (72) for evidence of damage. Replace items as necessary.

h. Inspect Bearing Guides (51) for excessive wear. Replace Guides if necessary.

i. Inspect Needle Bearings for roughness. Replace Bearings if necessary.

j. Inspect all parts for cleanliness. Clean parts with Isopropyl Alcohol or an approved equal.

5-5.2.3 Unit Reassembly (See Figure 6-2). Reassemble the Unit in the reverse order of numerical sequence of Item Numbers. During reassembly, the following precautions and procedures shall be observed.

a. When installing Eccentrics (85), make adjustment in accordance with paragraph 5-3.2.3.

b. When assembly Printed Circuit Board (74), Card Guide Assembly (73), Platen (78), and Sheet Insulator (75), if applicable, secure Screws (71) with Loctite fluid, AMP Part No. 23419-3.

c. When installing Entrance Lip (72), secure the three Screws (71) with Loctite fluid, AMP Part No. 23419-3.

d. When installing Card Insertion Switch (69), make adjustment in accordance with paragraph 5-3.2.2.

e. Secure Bearing Guides (51) to Platen (78) with Loctite fluid, AMP Part No. 23419-3, if removed.

f. During reassembly of Card Drive Assembly, apply one drop of general purpose light oil to bore of Segment Gear (58) and one drop to Stud Shaft (61). Rotate assembly several times to work in oil, then wipe off excess. Rotation of the Stud Shaft and Segment Gear must be free and the operation throughout the engaged circumference must be smooth.

g. If necessary to replace Spring Retainer (49), secure it to the bottom side of the Spring and Block Assembly (49) with Epoxy, AMP Part No. 1422071-8.

h. If necessary to remove, Card Stop (46), make adjustment in accordance with paragraph 5-3.2.5.

i. When installing Spring and Block Assembly (50) on Base (40) or Bars (41), secure Screws (38) with Loctite fluid, AMP Part No. 23419-3 after adjusting Assembly in accordance with paragraph 5-3.2.6.

j. Secure Base or Bars to Frame Sub Assembly (94) using the correct amount of Shims (35) at four places for proper Contact Spring deflection in accordance with adjustment procedure in paragraph 5-3.2.4.

k. When installing Card Read Switch (32), secure Screws (30) with Loctite fluid, AMP Part No. 23419-3, after making adjustment in accordance with paragraph 5-3.2.2.

l. Perform Unit checkout in accordance with paragraph 5-2.2.2.

m. Reinstall Unit in accordance with paragraph 5-2.2.4.

SECTION VI
PARTS LIST

This section contains the parts list for the Card Tester and card reader parts breakdown, with the exception of the parts breakdown for individual printed circuit boards. The parts lists for the printed circuit boards are located with the individual printed circuit board descriptions in section VIII. In the Card Tester and power supply parts lists, tables 6-2, 6-4 and 6-5, the manufacturers are identified by federal supply code numbers per cataloging H 4-2; a code-to-name cross reference index is provided in table 6-1. Complete parts listing of the card reader is provided in table 6-3 and exploded view illustrations of the reader are provided in figures 6-1 and 6-2. Power supply parts are listed in table 6-4..

Table 6-1 Index to Manufacturers Codes.

CODE	NAME	ADDRESS
00779	Amp, Inc.	P. O. Box 3608 Harrisburg, Pa.
01121	Allen-Bradley Co.	1201 S. 2nd Street Milwaukee, Wisconsin
01295	Texas Instruments, Inc. Semiconductor Components Div.	13500 North Central Expressway Dallas, Texas
04713	Motorola Semiconductor	505 East McDowell Phoenix, Arizona
06540	Amatom EleC. Hardware Co. Div. Mite Corp.	81 Rockdale Ave. New Rochelle, N.Y.

Table 6-1 Index to Manufacturers Codes (Cont'd)

CODE	NAME	ADDRESS
06809	Dynatronics	P.O. Box 2566 Orlando, Florida
07137	Transistor Electronics Corp. (also called TEC-Lite)	Hwy. 169-Co. Road 18 Minneapolis, Minnesota
07263	Fairchild Semiconductor	313 Bayshore Frontage Mountain View, California
14655	Cornell-Dubilier Electric Corp. (CDE)	50 Paris Street Newark, New Jersey
14949	Trompeter Electronics, Inc.	7238 Eton Avenue Canoga Park, California
35009	IRC Resistors	Ontario, Canada
70903	Belden Mfg. Co.	415 S. Kilpatrick Chicago, Illinois
71279	Cambridge Thermionic Corp.	445 Concord Avenue Cambridge, Mass.
71785	Cinch Mfg. Co. & Howard B. Jones Div.	1026 S. Homan Ave. Chicago, Illinois
75915	Littlefuse, Inc.	800 E. Northwest Hwy. Des Plaines, Illinois
80183	Sprague Product Co.	N. Adams, Mass.
80294	Bourns, Inc.	6135 Magnolia Avenue Riverside, California
81073	Grayhill, Inc	531 Hillgrove La Grange, Illinois
82389	Switchcraft, Inc.	5527 N. Elston Avenue Chicago, Illinois

Table 6-1 Index to Manufacturers Codes (Cont'd)

CODE	NAME	ADDRESS
86577	Precision Metal Products of Malden, Inc.	41 Elm Street Stoneham, Mass.
90201	P. R. Mallory Co., Inc.	Detroit, Michigan
94144	Raytheon Co. Industrial Components Div.	465 Centre Quincy, Mass.
	ECC Corporation	1010 Pamela Drive Euless, Texas 76039

Table 6- 2 Card Tester Parts List

REF DES	FIGURE/ INDEX	DESCRIPTION	MFG/ CODE	PART NO	QTY
	1-1 6-1	CARD TESTER, Model ICT-102 CARD READER, See Table 6-3 (A-MP) REF. SCO-549-1	06809 00779	00-001436-1 04-001196-1	1
A1		PRINTED CIRCUIT CARD, Clock Generator	06809	08-890710-1	1
A2		PRINTED CIRCUIT CARD, Function Generator	06809	08-890711-1	1
A3		PRINTED CIRCUIT CARD, GO/NO- GO LOGIC	06809	08-890712-1	1
A4 A5		PRINTED CIRCUIT CARD, Programmable Driver	06809	08-890714-1	2
A6		PRINTED CIRCUIT CARD, Input Level Shifter	06809	08-890716-1	1
A7		PRINTED CIRCUIT CARD, Input Fault Generator	06809	08-890715-1	1
A8		PRINTED CIRCUIT CARD, Resistive Loads, 3K ohm	06809	08-890713-	1
A9		PRINTED CIRCUIT CARD, Resistive Loads, .510 ohm	06809	08-890713-2	1
DS1	3-1	LAMP, Indicator, green lens BULB, incandescent, clear, 14 volt, 80 MA, #382	07137	RDL-A1(F5-382)	1
DS2	3-1	LAMP, Indicator, red lens BULB, incandescent, clear, 14 volt, 80 MA, #382	07137	RDL-A1(F1-382)	1
J1	3-1	CONNECTOR, Audio Jack	82389	52B	1
J2	3-1	CONNECTOR, Receptacle, BNC, isolated	14949	BJ-27	1

Table 6-2. Card Tester Parts List (Cont'd)

REF DES	FIGURE/ INDEX	DESCRIPTION	MFG/ CODE	PART NO.	QTY
J3	3-1	CONNECTOR, PC Card Test Receptacle Assembly Receptacle, Blue, 56 pin	06809 00779	00-001437-1 67768-1	1
PSI	2-1	POWER SUPPLY, ASSEMBLY See Table 6-4	06809	00-001435-1	1
S1	3-1	SWITCH, Momentary Contact Red Lens Bulb, incandescent, clear 14 volt, 80 MA, #382	07137	RBL-43L-A- (1-382)	1
S2	3-1	SWITCH, ROTARY, 10 position 7 deck, 36° Index KNOB, Round Bar, Dial Skirted, Matte	81073 94144	43A36-7-1-10N 70B-3-2G	1 1
S3	3-1	SWITCH, Rotary, 10 position 8 deck, 36° Index KNOB, Round Bar, Dial Skirted, Matte	81073 94144	42A36-8-1-1CN 70B-3-2G	1 1
S4, S5	3-1	SWITCH, Rotary, 12 position, 5 deck, 30° Index KNOB, Round Bar, Dial Skirted, Matte	81073 94144	44A30-5-1-12N 70B-3-2G	2 2
S6	3-1	SWITCH, Momentary Contact Blue lens Bulb, incandescent, clear, 14 volt, 80 MA, #382	07137	RBL-43L-A (6-382)	1
TP1 TP26	3-1	TEST POINT, White, Tip Jack	94144	TJ-408W	26
TP27	3-1	TEST POINT, Black, Tip Jack	94144	TJ-405BL	1
		CONNECTOR Plug In Assembly (Mates with Power Supply)	06809	01-002622-1	1
		ADAPTER Plug Card	06809	08-890697-1	1

Table 6-3 Card Reader Parts List

The Parts List begins with the top assembly, then itemizes all Sub Assemblies and detail parts numerically in the preferred order of disassembly. Missing part numbers do not pertain to the model.

The Part Nomenclature for assemblies, sub-assemblies and detail parts are indented under the next higher assembly on which they are used.

The Number Required column indicates the quantity of item required for the next higher assembly. Refer to figures 6-1 and 6-2 for part locations.

ITEM NO.	AMP PART NUMBER	DESCRIPTION	NO. REQ.
1	00-001463	Card Reader (AMP Model 5-426890-5	
2 1	426735-1	Frame Sub-Assy. Card Drive	1
3	22-887-6	Washer, #10 Plain Flat	4
4	22873-5	Washer, #10 Spring Lock	4
5	22684-1	Screw #10-34 x .5 lg. Slot Pan Hd.	4
6	426755-1	Bracket Mtg. (L.H. Panel)	1
7	426755-2	Bracket Mtg. (R.H. Panel)	1
8	3-21119-6	Pin, Slotted Spring .094dia. x .500 lg	1
9	426807-1	Handle	1
10		Not Used	
11		Not Used	
12		Not Used	
13		Not Used	
14		Not Used	
15		Not Used	

Table 6-3 Card Reader Parts List (Cont'd)

ITEM NO.	AMP PART NUMBER	DESCRIPTION	NO REQ
16		Not Used	
17		Not Used	
18		Not Used	
19		Not Used	
20		Not Used	
21		Not Used	
22		Not Used	
23		Not Used	
24		Not Used	
25		Not Used	
26		Not Used	
27		Not Used	
28		Not Used	
29		Not Used	
30	2-22798-4	Screw, #2-56 x .375 lg. Slot Pan Hd.	2
31	426771-1	Spacer, Switch	1
32	426748	Switch, Card Read	1
33	22873-5	Washer, Spring Lock #10	4
34	22031-2	Screw, #10-24 x .500 lg. Cap	4
35	426754-1	Shim, laminated	4

Table 6-3 Card Reader Parts List (Cont'd)

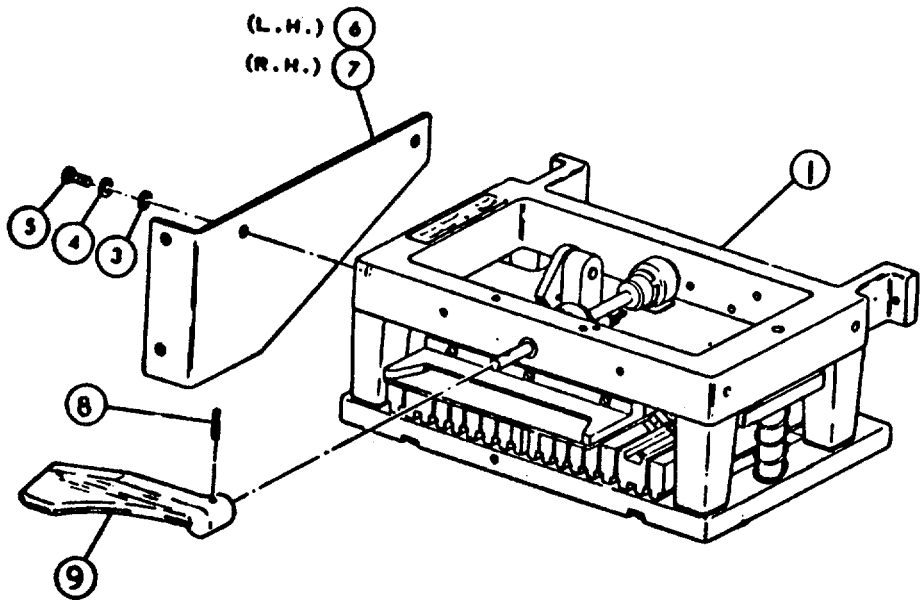
ITEM NO.	AMP PART NUMBER	DESCRIPTION	NO. REQ.
36	426776-1	Spring, Feed Roller Loading	1
37	426773-1	Pin, Card Reader	1
38	1-21081-5	Screw, #8-32 x .625 lg. Soc. Hd. Cap	4
39	21105-4	Pin, Dowel .125 dia. x .750 lg.	2
40		Not Used	
41A	426715-1	Bar Mounting (rear)	1
41B	426715-2	Bar Mounting (front)	1
42		Not Used	
43	22887-2	Washer, #4 Plain Flat	2
44	22873-2	Washer, #4 Spring Lock	2
45	4-22798-3	Screw, #4-40 x .315 LG. Slot Pan Hd.	2
46	426753-1	Stop, Card	1
47	2-22282-7	Spring Compression	4
48	2-21989-4	Screw Shoulder Soc. Hd.	4
49	426774-1	Retainer, Spring	1
50	426985-1	Spring & Block Assy. Contact	1
51-	426713-2	Guide Bearing	2
52	1-22286-5	Spring Extension	1
53	4-22798-3	Screw #4-40 x .315 lg. Slot Pan Hd.	2
54	426906-1	Shim, Card Drive	AIR

Table 6-3 Card Reader Parts List (Cont'd)

ITEM NO.	AMP PART NUMBER	DESCRIPTION	NO REQ.
55	23811-1	Ring, "O"	1
56	1-21112-5	Ring, Retaining	1
57	1-22183-5	Pin, Grooved Type 67	1
58	426721-4	Gear Segment	1
59	426734-1	Wheel Drive	1
60	426731-1	Shaft Assy.	1
61	426729-2	Shaft, Stud	1
62	426720-1	Housing Gear Shafts	1
63		Not Used	
64		Not Used	
65	21124-4	Nut, #2-56 UNC-2B Hex	2
66	22873-1	Washer, Spring Lock #2	2
67	22887-2	Washer Flat #2	2
68	2-22798-4	Screw #2-56 x .375 lg. Slot Pan Hd.	2
69	426195-1	Switch, Card Insertion	1
70	426756-1	Actuator, Insertion Switch	1
71	2-22798-4	Screw #2-56 x .375 lg. Slot Pan Hd.	9
72	426768-1	Lip Entrance	1
73	426959-1	Guide Assy., Card	1
74	1-427105-8	Board Printed Circuit (Bussed Row)	1

Table 6-3 Card Reader Parts List (Cont'd)

ITEM NO.	AMP PART NUMBER	DESCRIPTION	NO. REQ.
75	426898-1	Sheet Insulator	1
76	1-22183-6	Pin, Grooved .125 x .500 lg.	1
77		Not Used	
78	426739-1	Platen, Machined	1
79	3-21119-8	Pin, Slotted Spring	1
80		Not Used	
81	3-21012-9	Screw, Soc. Set #8-32 x .188 lg.	2
82	426746-1	Washer Nylon	2
83	23.717-6	Ring, Retaining	4
84	1-23507-0	Bearing, Needle	2
85	426739-1	Eccentric	2
86	426740-1	Shaft, Actuation	1
87		Not Used	
88	21119-4	Pin, Slotted Spring .062 x .375 lg.	2
89	395725-1	Tag, Name	1
90	23507-9	Bearing, Needle	1
91	4-21119-0	Pin, Slotted Spring .094 dia. x .750 lg	2
92	2-21105-9	Pin, Dowel	2
93	21105-4	Pin, Dowel	3
94	426792-2	Frame, Machined	1



Notes:

1. Card reader purchased from AMP Inc. Harrisburg, Pa. AMP Model number 2981A
   As modified per Dynatronics specification 04-001196.

Figure 6-1. Card Reader Exploded View

Table 6-4 Power Supply Parts List (figure 6-3)

REF DES	FIGURE/ INDEX	DESCRIPTION	MFG/ CODE	PART NO.	QTY
A1		PRINTED CIRCUIT BOARD, Assembly (see table 6-5)	06809	08-890647-1	1
C16	6-3	CAPACITOR, 15000 MF, 15WVDC 1 3/4 in. Dia.	90201	CGS153UO15U 2C3PH	1
C17	6-3	CAPACITOR, 4700 MF, 25WVDC 1 3/8 in. Dia.	90201	CGS472U025 R2C3PH	1
C18-C20	6-3	CAPACITOR, 4900 MF, 50 WVDC 2 in. Dia.	90201	CGS492U05OV 2C3PH	3
C21	6-3	CAPACITOR, .047 micro-farad 400 WVDC	06809	20-000003	1
Fl	6-3	FUSE, 2 amp, 3AG	75915	313002	1
F2	6-3	FUSE, 3/4 amp, 3AG	75915	312.750	1
Q12	6-3	TRIAC, THERMOTAB, 3-16 AMP	E88Rp	A01122	1
R69	6-3	RESISTOR, 2.2K ±5%, 1/2W	35009	RC20GF222J	1
R70	6-3	RESISTOR, 10K ±5%, 2'N	35009	RC42GF103J	1
R71A R71B	6-3	RESISTOR, Composition, 10 OHM. 1W, ±5%	35009	RC32GF100J	2
T1	6-3	TRANSFORMER.	06809	04-001225-1	1
XF1, XF2	6-3	FUSE HOLDER, 3AG	75915	342014	2
P1	6-3	PLUG, 2 pin	71785	P-302-CCT	1
J1	6-3	SOCKET, 2 pin	71785	S-302-AB	1
		POWER CORD, W/PLUG, 8 feet long	70903	172375	1

Table 6-5. Printed Circuit Board (A1) Parts List (See figure 6-4)

REF DES	FIGURE/ INDEX	DESCRIPTION	MFG/ CODE	PART NO.	QTY
AR1-AR5	6-4	PRECISION VOLTAGE REGULATOR	07263	U5R7723393	5
C1, 2, 9	6-4	CAPACITOR, .1UF 16V	80183	HY450	3
C3, 5, 7, 11, 13	6-4	CAPACITOR, 560 PF	80183	CK05BX561K	5
C4, 6	6-4	CAPACITOR, 100 UF, 7V	14655	UHL100-7	2
C8, 12, 14	6-4	CAPACITOR, 50 UF, 20V	14655	UHL50-20	3
C10, C22	6-4	CAPACITOR, 390 UF, 20V	14655	UHL390-20	2
CR1-18	6-4	DIODE, RECTIFIER	01295	IN4002	18
CR19-24	6-4	DIODE, SIGNAL	01295	IN4454	6
E1-22 26	6-4	TERMINAL POST	86577	SS-5670	23
Q1-Q2	6-4	TRANSISTOR, PLASTIC, PWR, NPN	04713	2N4441	2
Q3, 4, 6	6-4	TRANSISTOR, PLASTIC, PWR, NPN	04713	MJE3055	3
Q5, Q10	6-4	TRANSISTOR, PLASTIC, PWR PNP	04713	MJE2901	2
Q7, 8, 9	6-4	TRANSISTOR, NPN (SELECTED PER 04-001266)	04713	MJE3055	3
Q11	6-4	TRANSISTOR, NPN (T018)	04713	2N2222A	1
R1, R9	6-4	RESISTOR, MET. FILM, 1.0K 1/8W, ±1%	35009	RN55D1001F	2
R2, 16, 43, 61	6-4	POTENTIOMETER, 1K, OHMS	80294	3250P-1-102	4
R3, R1l	6-4	RESISTOR, 3.O1K OHMS, 1/8W, ±1%	35009	RN55D3011F	2

Table 6-5. Printed Circuit Board (A1) Parts List (See figure 6-4) (Cont'd)

REF DES	FIGURE/ INDEX	DESCRIPTION	MFG/ CODE	PART NO.	QTY
R4, R12	6-4	RESISTOR, 1.2K OHMS, 1/4W ±5%	35009	RC07GF122J	2
R5, 13, 29, 48, 66	6-4	RESISTOR, 330 OHMS, 1/4W, ±5%	3.5009	RC07GF331J	5
R6, R14	6-4	RESISTOR, 0.39 OHMS, 2W, ±10%	35009	19-000009-1	2
R7	6-4	RESISTOR, 180 OHMS, 1/4W, ±5%	35009	RC07GF181J	1
R8, 30, 47	6-4	RESISTOR, 270 OHMS, 1/4W, ±5%	35009	RC07GF271J	3
R10	6-4	POTENTIOMETER 1K	80294	3305P-1-102	1
R15, 42 60	6-4	RESISTOR, 4.64K, 1/8W, ±1%	01121	RN55D4641F	3
R17, 44, 62	6-4	IRESISTOR, 1.50K, 1/8W, ±1%	01121	RN55D1501F	3
R18, 45 63	6-4	RESISTOR, 6.04K, 1/8W, ±1%	01121	RN55D6041F	3
R19, 46 64	6-4	POTENTIOMETER, 10K OHMS	80294	3250-1-103	3
R20, .33 51	6-4	RESISTOR, 4.02K, 1/8W, ±1%	01121	RN60C4021F	3
R21, 35, 54	6-4	RESISTOR, 634 OHMS, 1/10W, ±I%	01121	RN55C6340F	3
R22, 34, 52	6-4	RESISTOR, 1.27K, 1/10W, ±1%	01121	RN55C1271F	3
R23 36, 53	6-4	RESISTOR, 2.55K, 1/10W, ±1%	01121	RN55C2551F	3

Table 6-5.. Printed Circuit Board (Al) Parts List (See figure 6-4) (Cont'd)

REF DES	FIGURE/ INDEX	DESCRIPTION	MFG/ CODE	PART NO.	QTY
R24, 37 55	6-4	RESISTOR, 5.11K, 1/10W, ±1%	01121	RN55C5111F	3
R25, 38 56	6-4	RESISTOR, 10.2K, 1/8W, ±1%	01121	RN55D1022F	3
R26, 39 57	6-4	RESISTOR, 20.5K, 1/8W, ±1%	01121	RN55D2052F	3
R27, 40 58	6-4	RESISTOR, 39K OHMS, 1/4W, ±5%	01121	RC07GF393J	3
R28, 41 59	6-4	RESISTOR, 82K OHMS, 1/4W, ±5%	01121	RC07GF823J	3
R31, 49 67	6-4	RESISTOR, 0.47 OHMS, 2W, ±10%	35009	19-000009-2	3
R32, 50	6-4	RESISTOR, 560 OHMS, 2W ±5%	01121	RC42GF561J	2
R65	6-4	RESISTOR, 15K, 1/4W, ±5%	01121	RC07GF153J	1
R68	6-4	RESISTOR, 100 OHMS, 1/4W, ±5%	01121	RC07GF101J	1
VRI-VR2	6-4	ZENER DIODE 5.6V	01295	IN752A	2
VR3	6-4	ZENER DIODE 13V	01295	IN964B	1
VR4	6-4	ZENER DIODE 6.8V	01295	IN754A	1

SECTION VII

DRAWINGS

7-1 INTRODUCTION.

This section contains the block, logic, and schematic drawings for the Card Tester with the exception of the drawings for the printed circuit cards which are located in section VIII of this manual. An explanation on the use of the drawings is provided below. Table 7-1 is an index to the drawings.

7-2 USE OF DRAWINGS.

7-2.1 LOGIC TERMINOLOGY AND DEFINITIONS. In the logic descriptions within this manual, the convention has been established of designating the relatively positive logic level (usually +3.5 volts) as "high", and the relatively negative logic level (usually 0 volts) as "low". These two terms can be readily correlated with the active-state level indicators (circles) used on logic symbols per MIL-STD-806B. The presence of a circle indicates that a low level activates the logic function; absence of a circle indicates that a high level activates the logic function. Since some logic elements used in the equipment are activated by low levels and others by high levels, the active-state indicators will vary from symbol to symbol. Both inverting and non-inverting elements are used and inversions are evidenced by the active-state level indicators.

Where applicable, signal names are prefixed by a "+" or "-" symbol which indicates the logic level when the name function is true. A "+" indicates a true high level and a "-" indicates a true low level.

7-2.2 STANDARD LOGIC SYMBOLS. Symbols for logic elements used in this equipment are in accordance with MIL-STD-806B. The logic elements are packaged on printed circuit cards, therefore, the appropriate logic symbols are

illustrated with the printed circuit card information in section VIII of this manual.

7-2.3 LOGIC CIRCUIT TAGGING LINES. The logic diagrams illustrate the logical operation of the circuits with all signal paths, and in addition, identify hardware used, physical location, pin numbers, and test point numbers. Figure 7-1 shows an example of a typical logic circuit and the identification system used thereto.

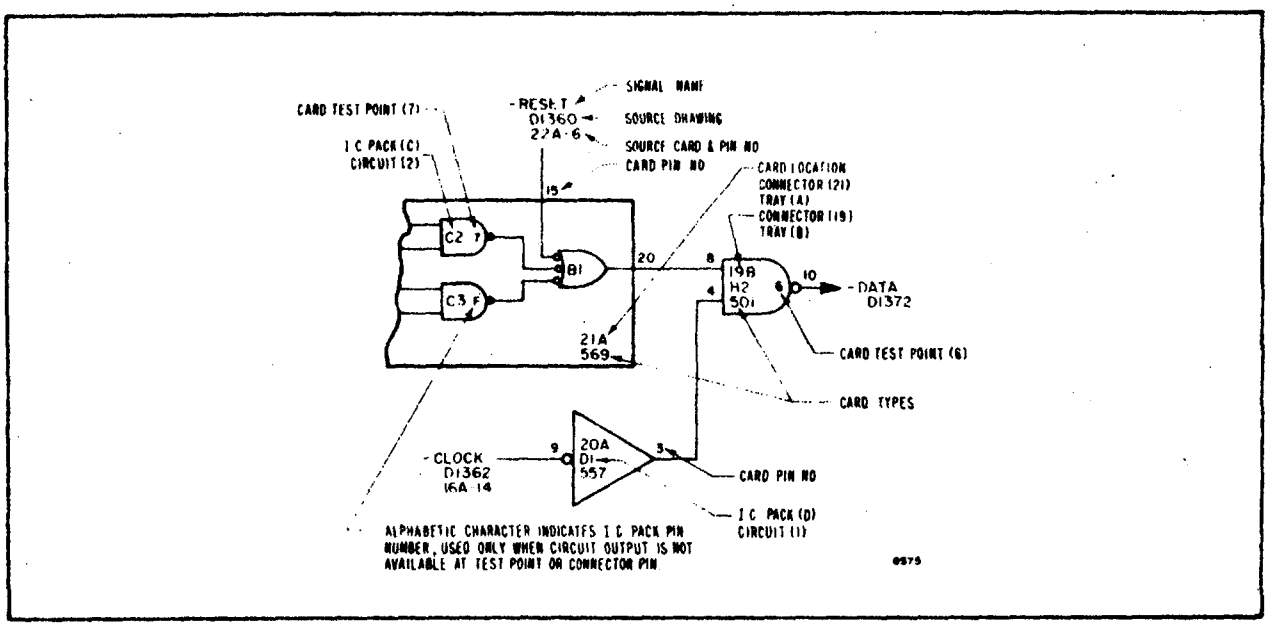


Figure 7-1. Typical Logic Circuit

Table 7-1 Drawing Index

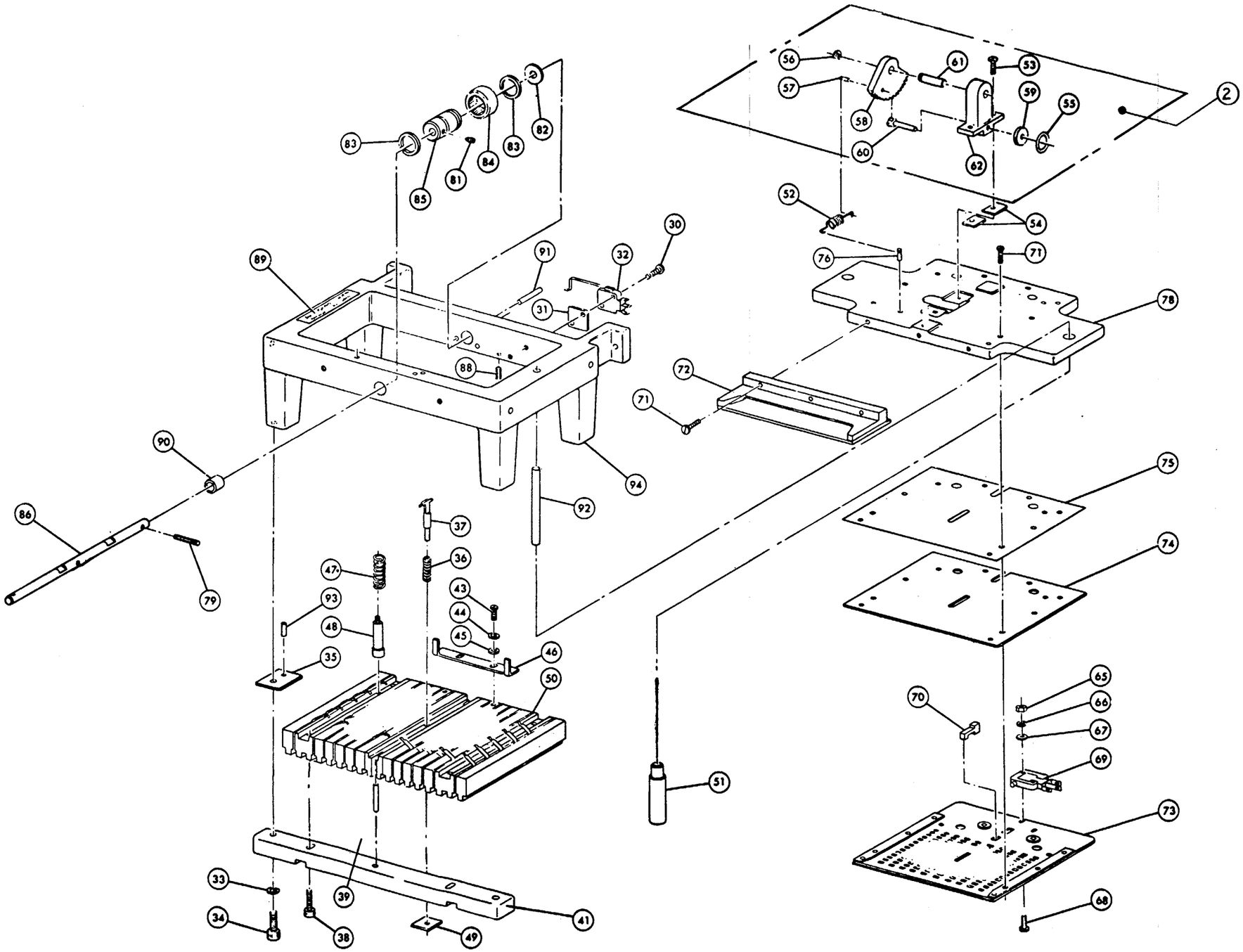
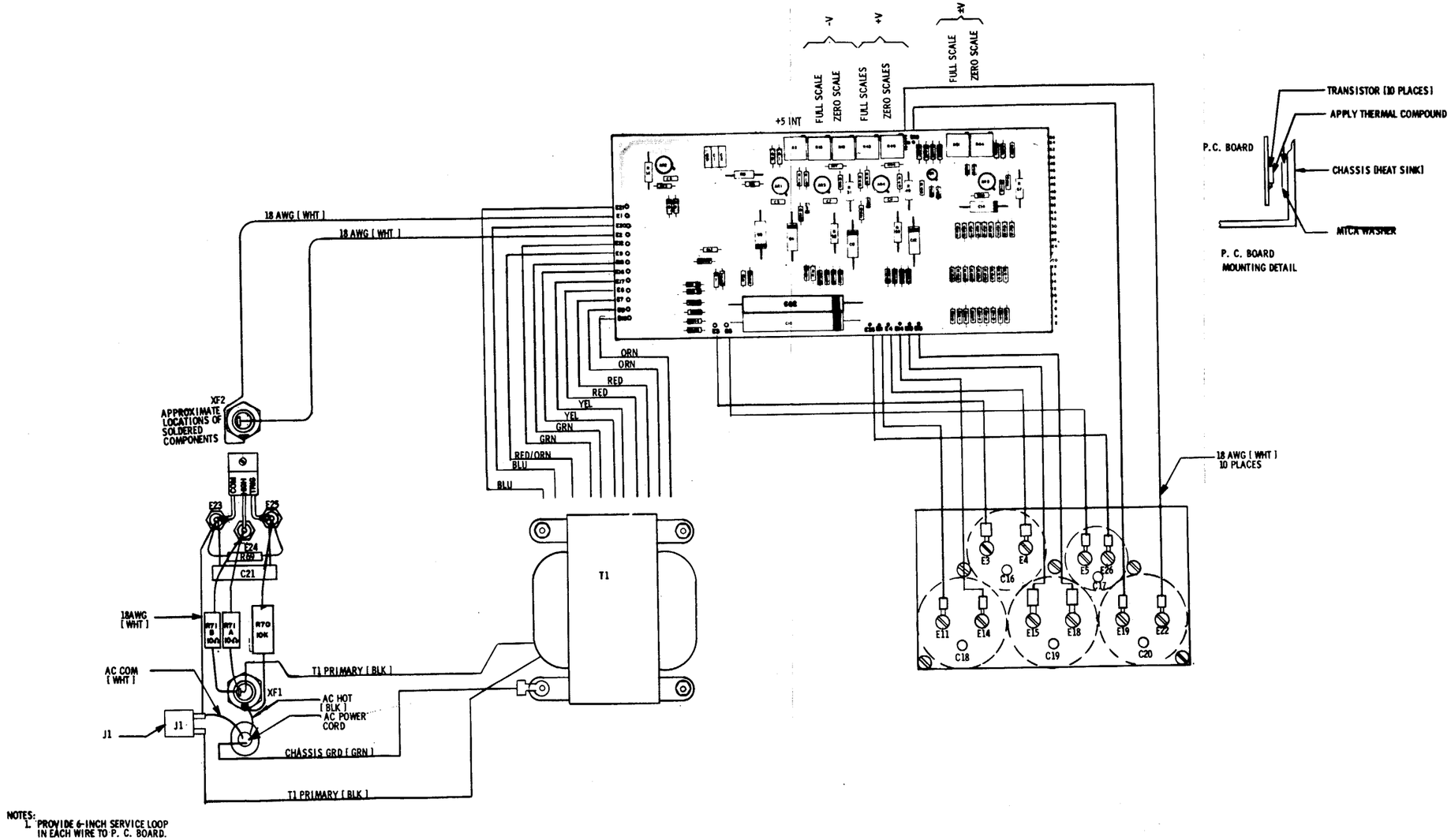


Figure 6-2. Card Reader Detailed Exploded View



02-003012-1

Figure 6-3. Power Supply Assembly

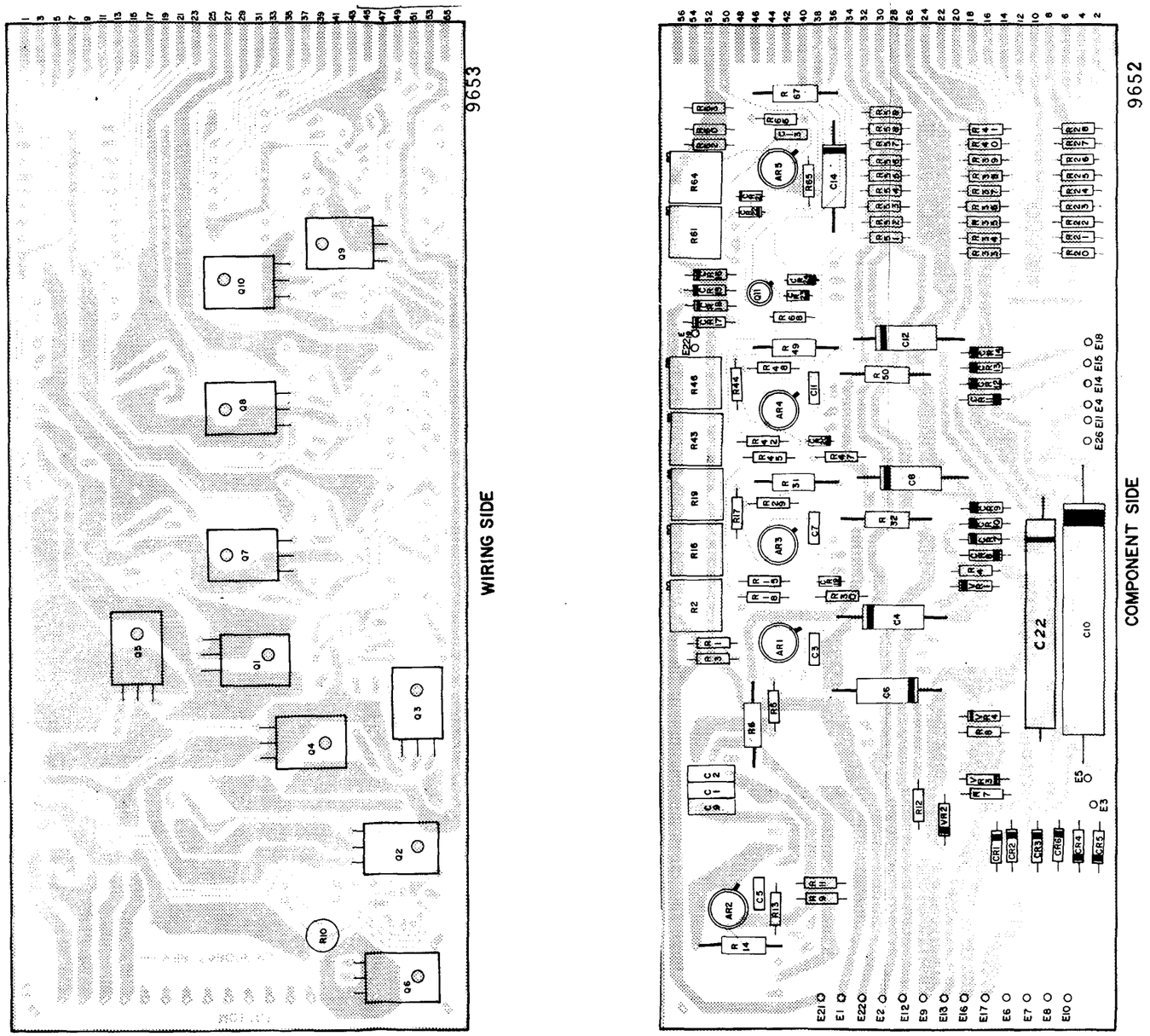
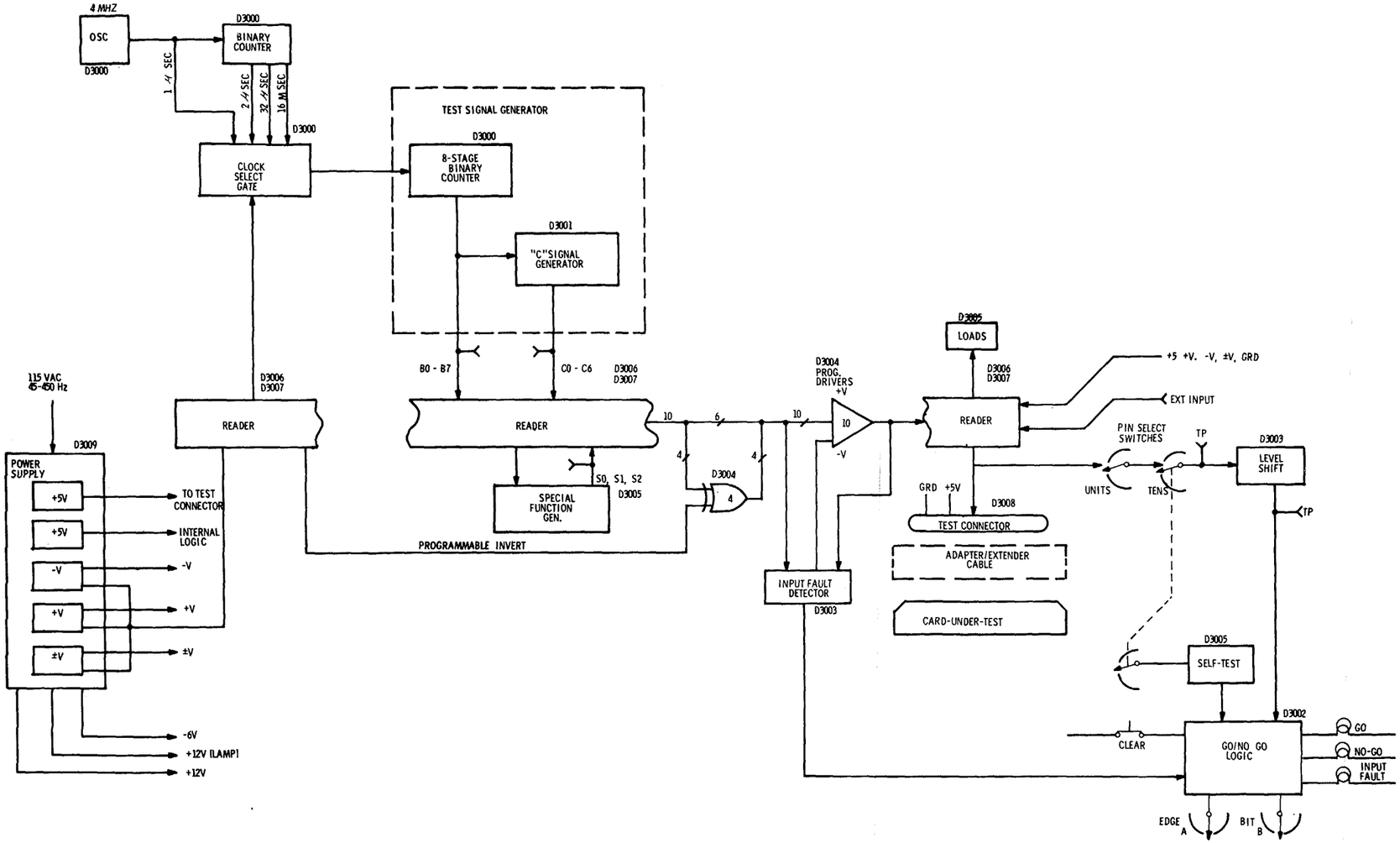
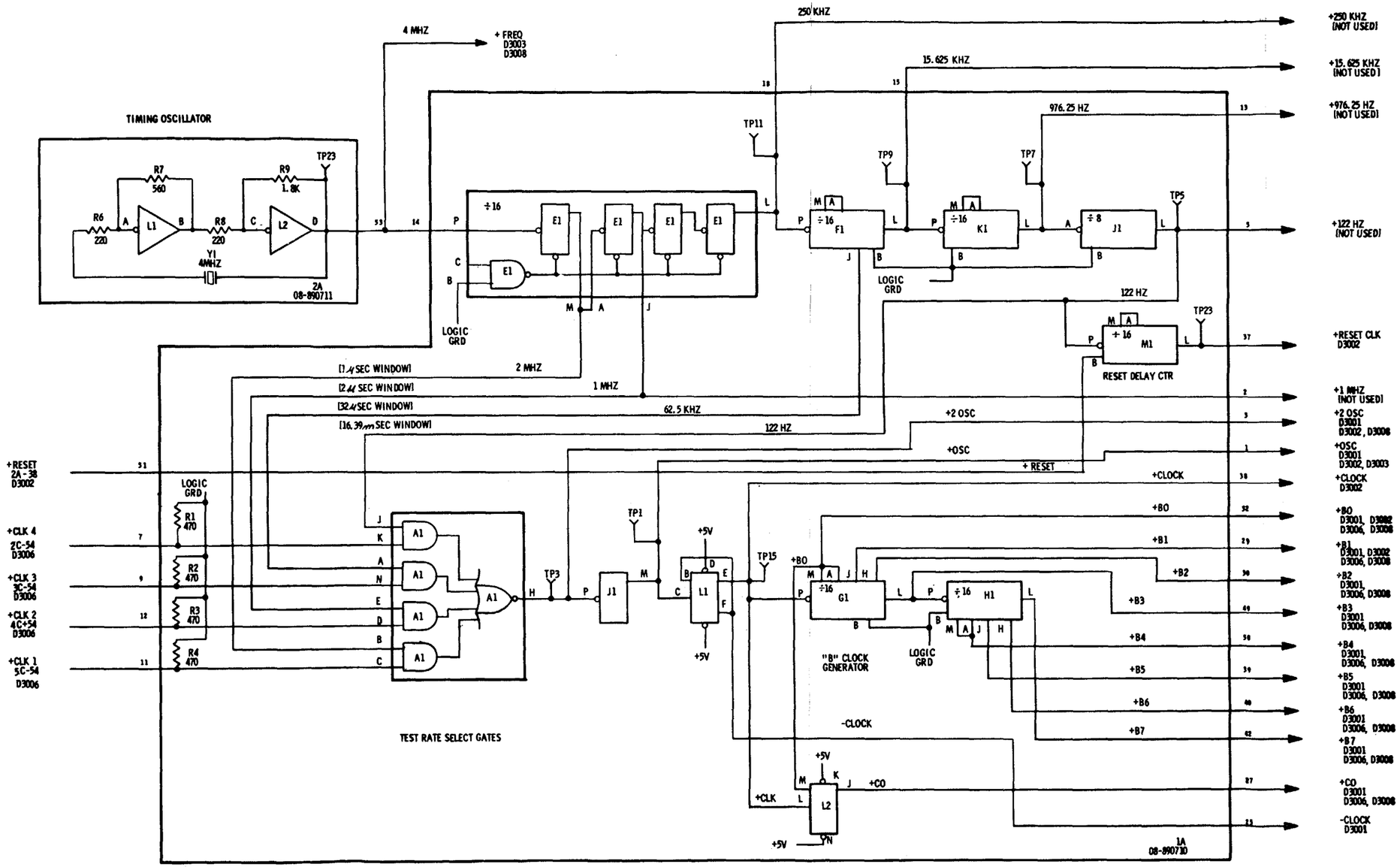


Figure 6-4. Assembly A1 Component Location



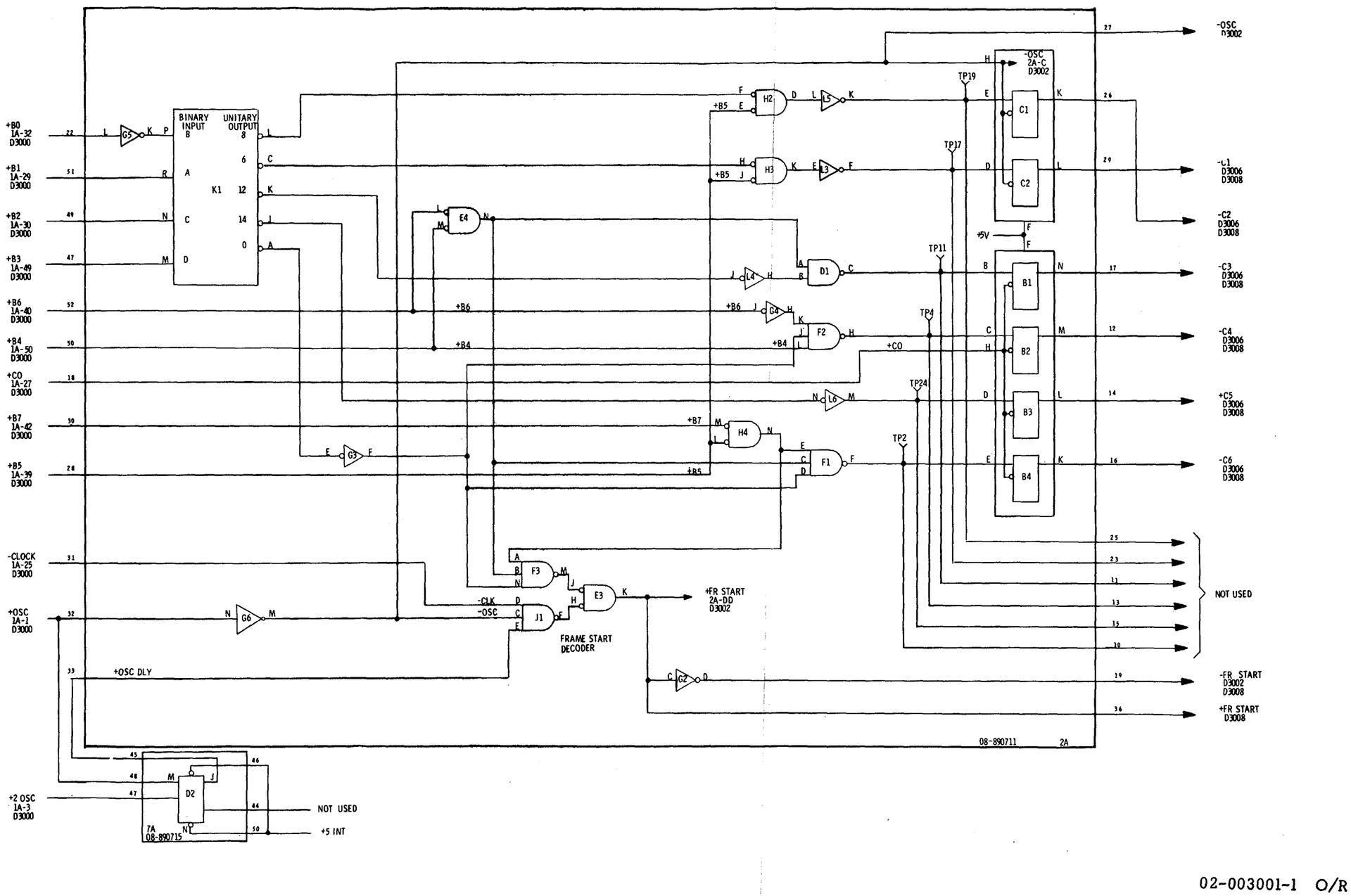
02-002999-1 O/R

Figure 7-2. Card Tester, Block Diagram



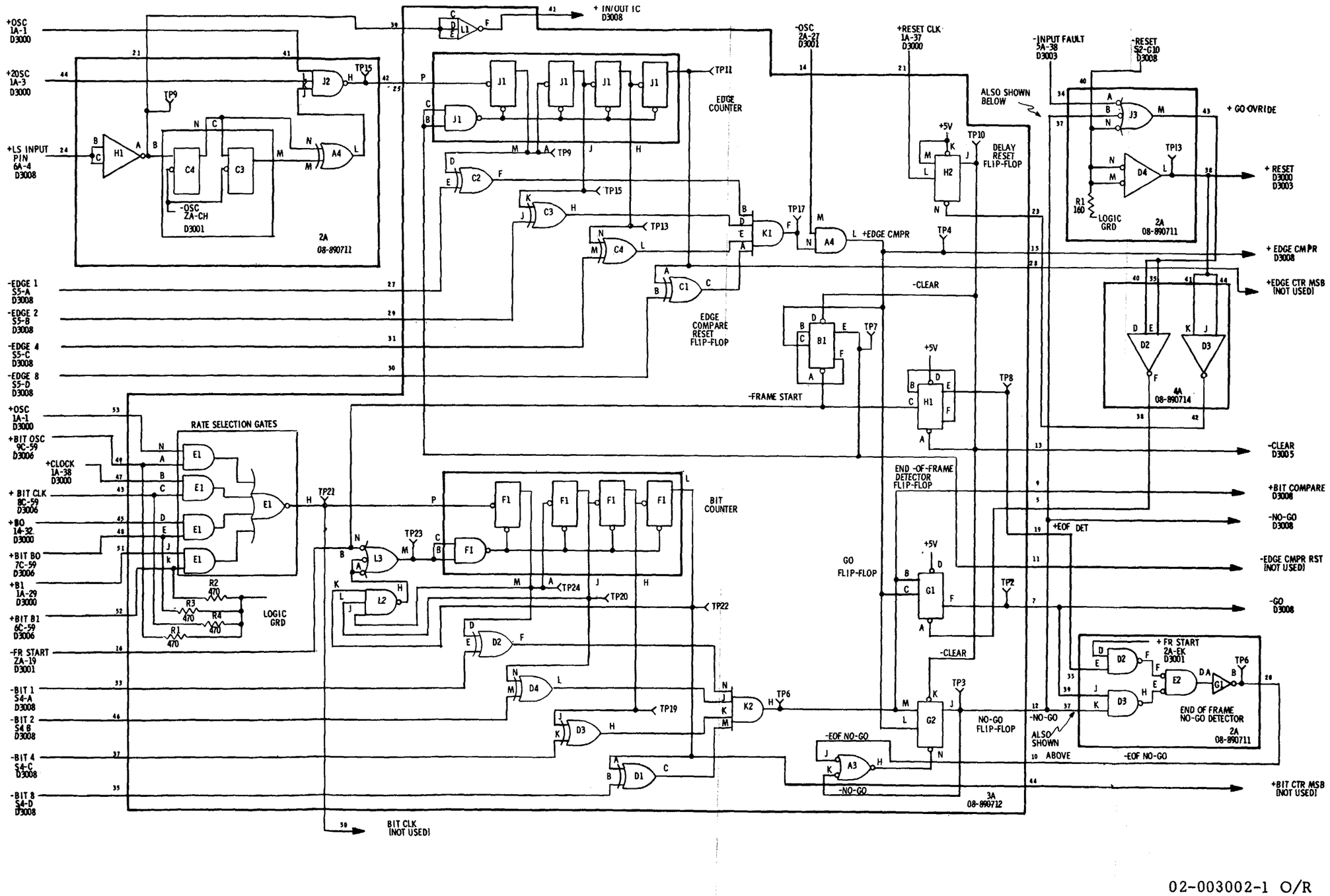
02-003000-1 O/R

Figure 7-3. "B" Clock Generator, Logic Diagram



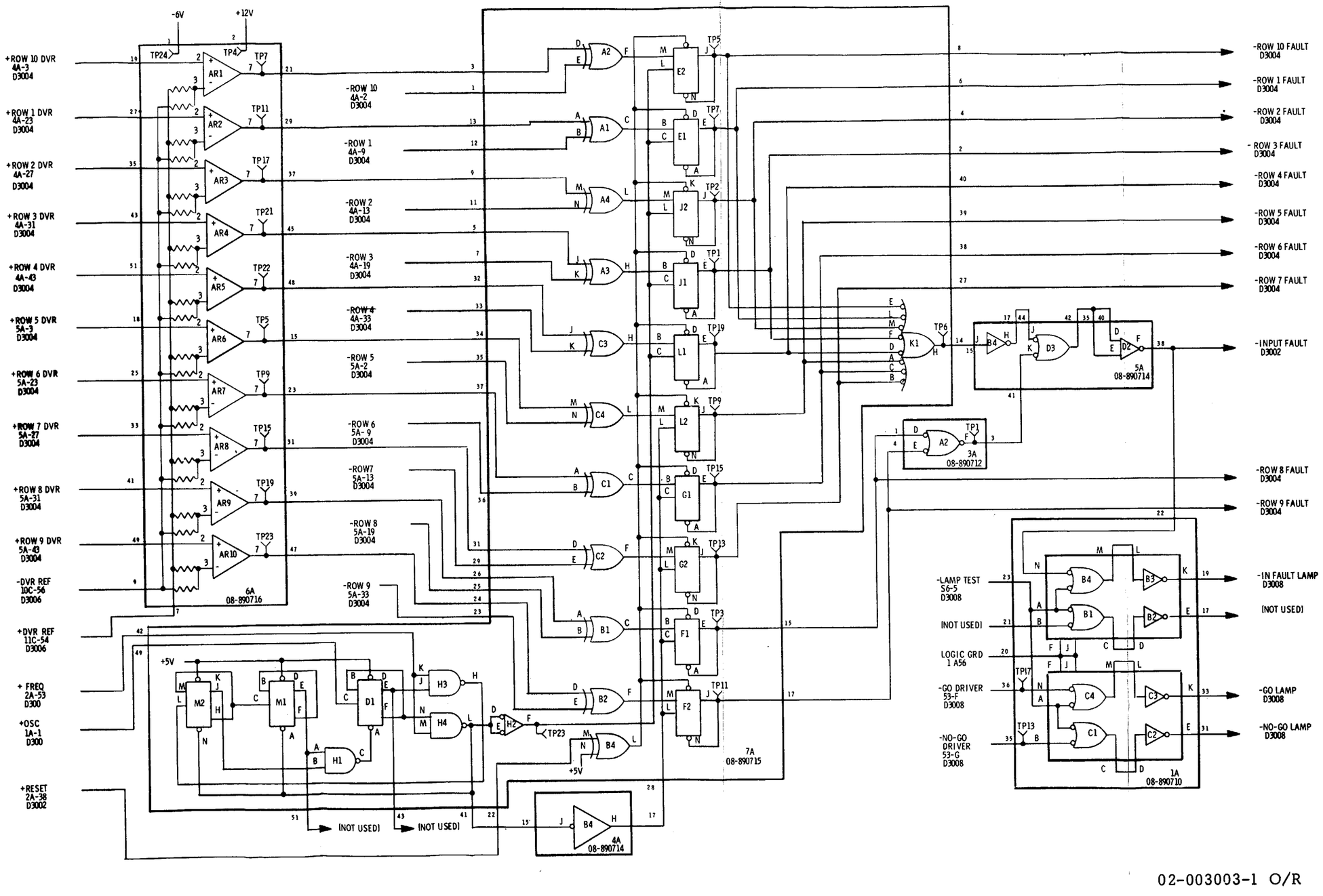
02-003001-1 O/R

Figure 7-4 "C" Clock generator, Logic Diagram
7-9/7-10



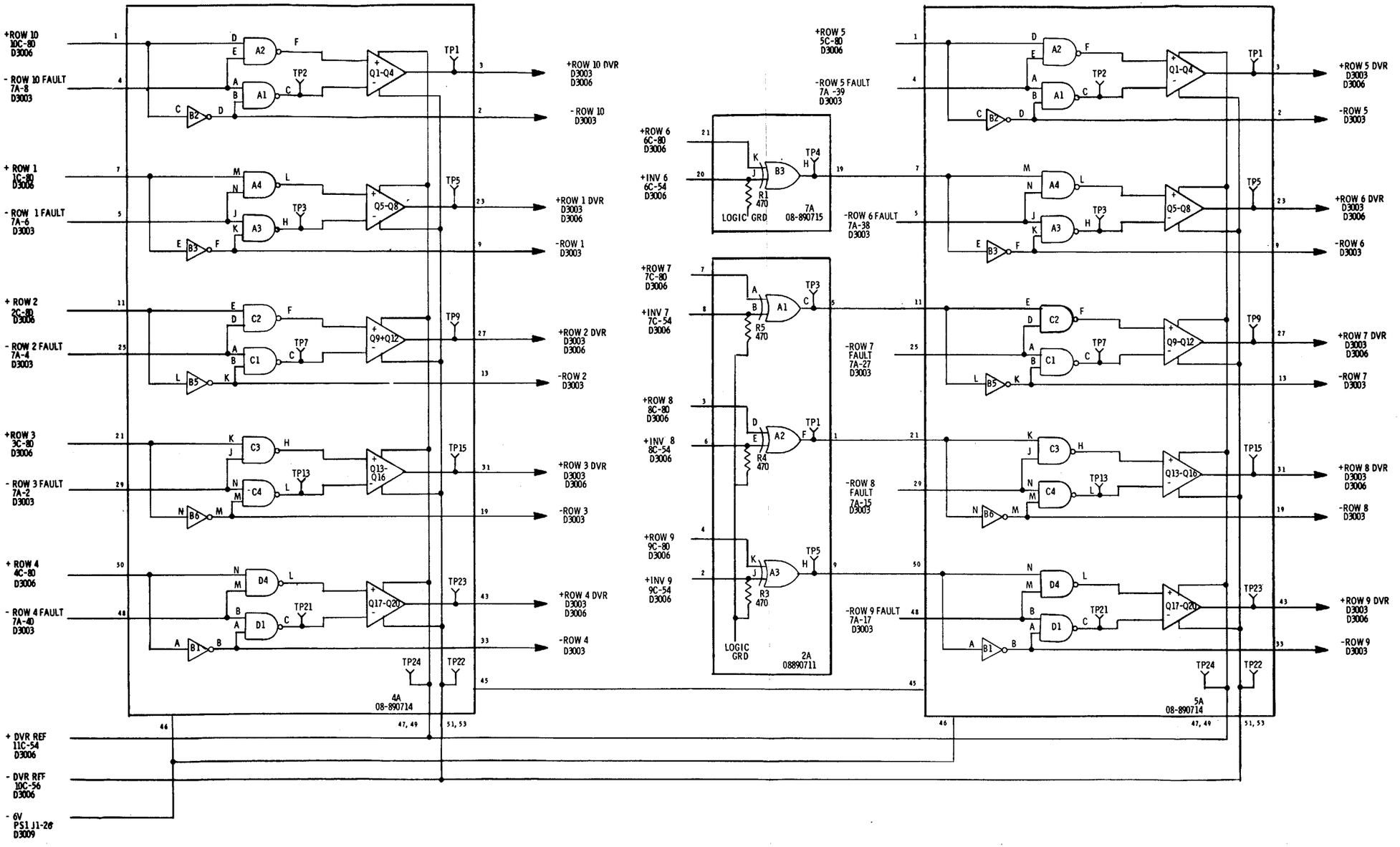
02-003002-1 O/R

Figure 7-5 GO/NO-GO Test Logic, Logic Diagram
7-11/7-12



02-003003-1 O/R

Figure 7-6 Input Fault Comparator, Logic diagram



02-003004-1 O/R

Figure 7-7 programmable Drivers, Logic Diagram

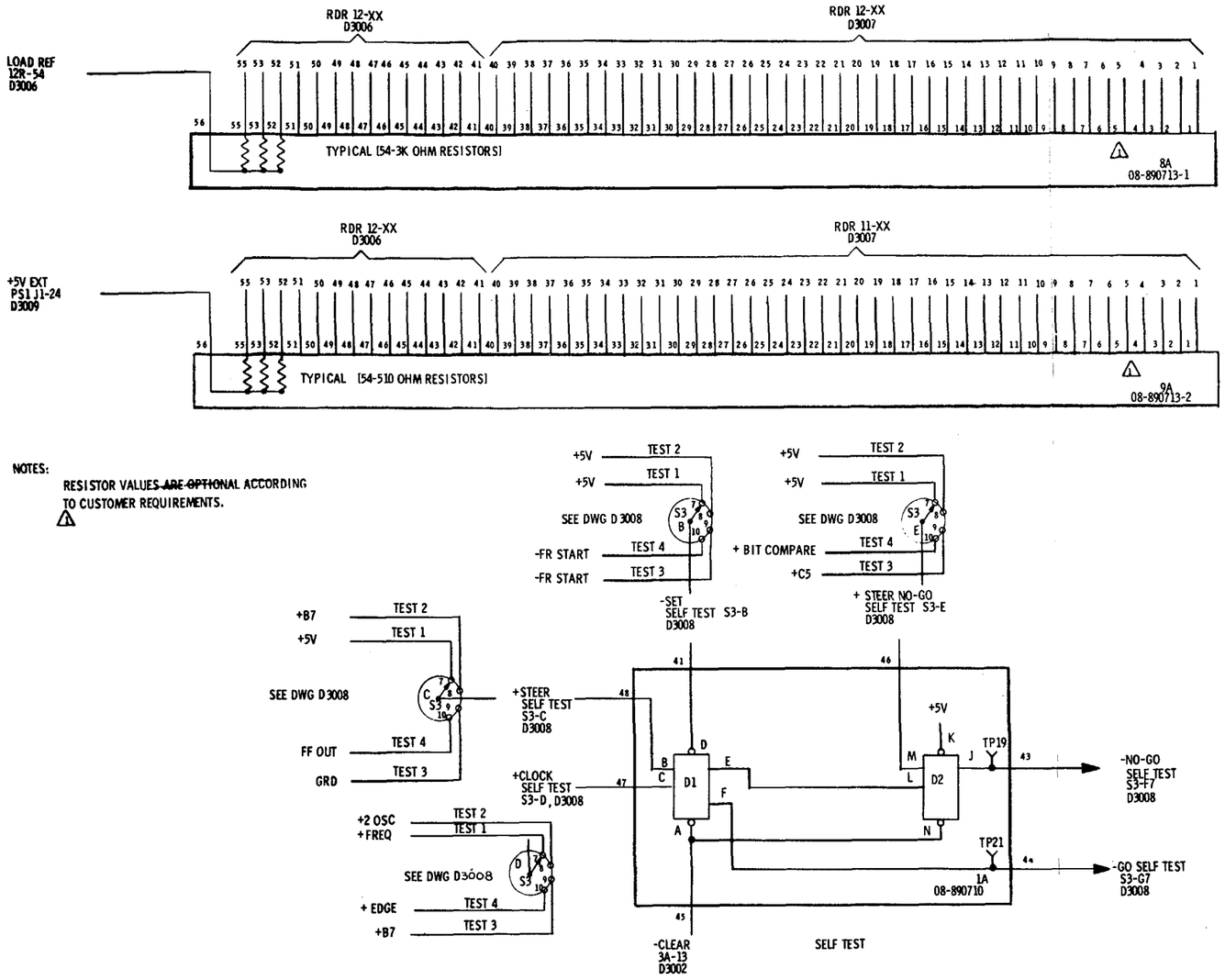


Figure 7-8 Self test, Programmable Functions, Spares and Load Resistor, Logic Diagram

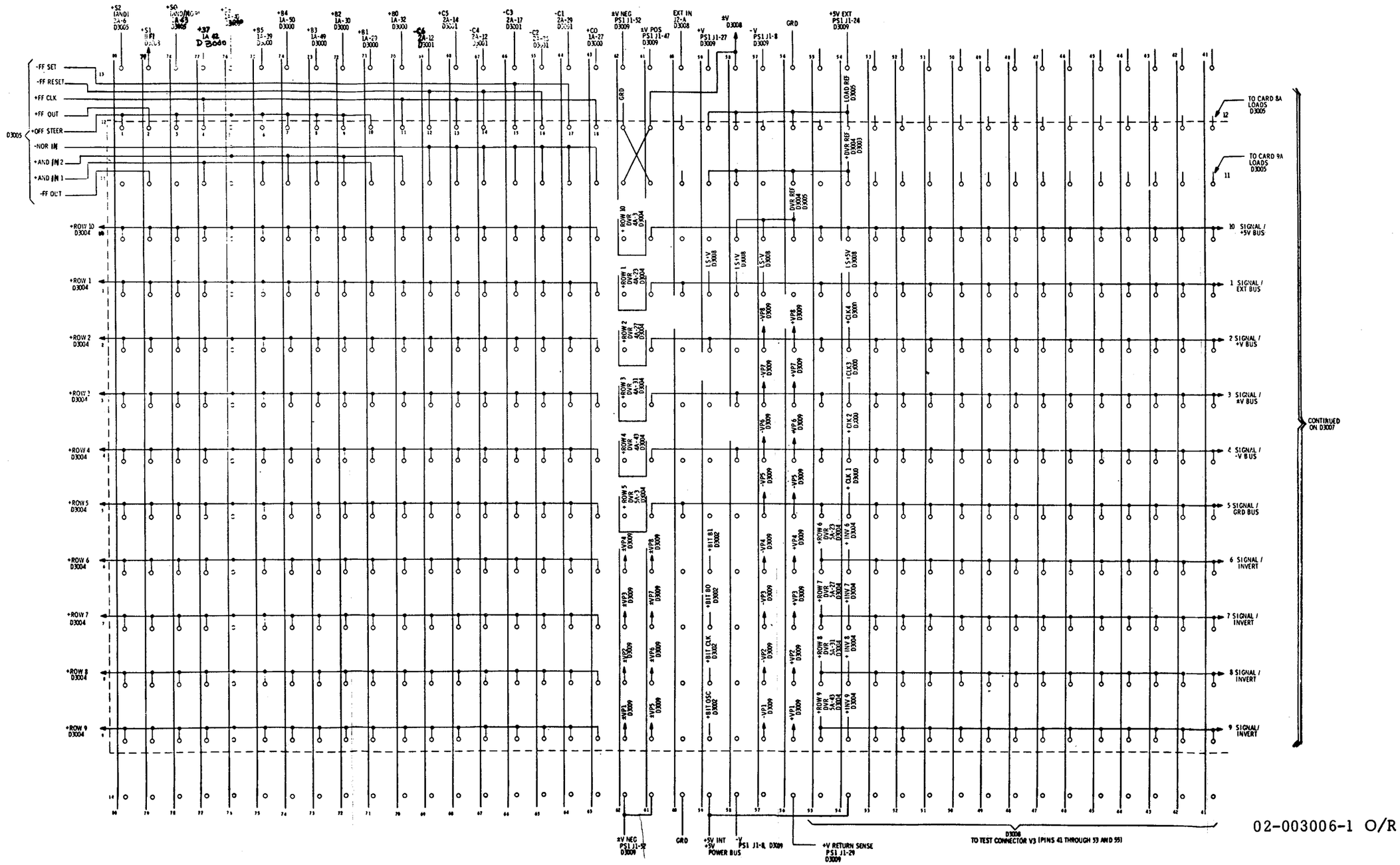
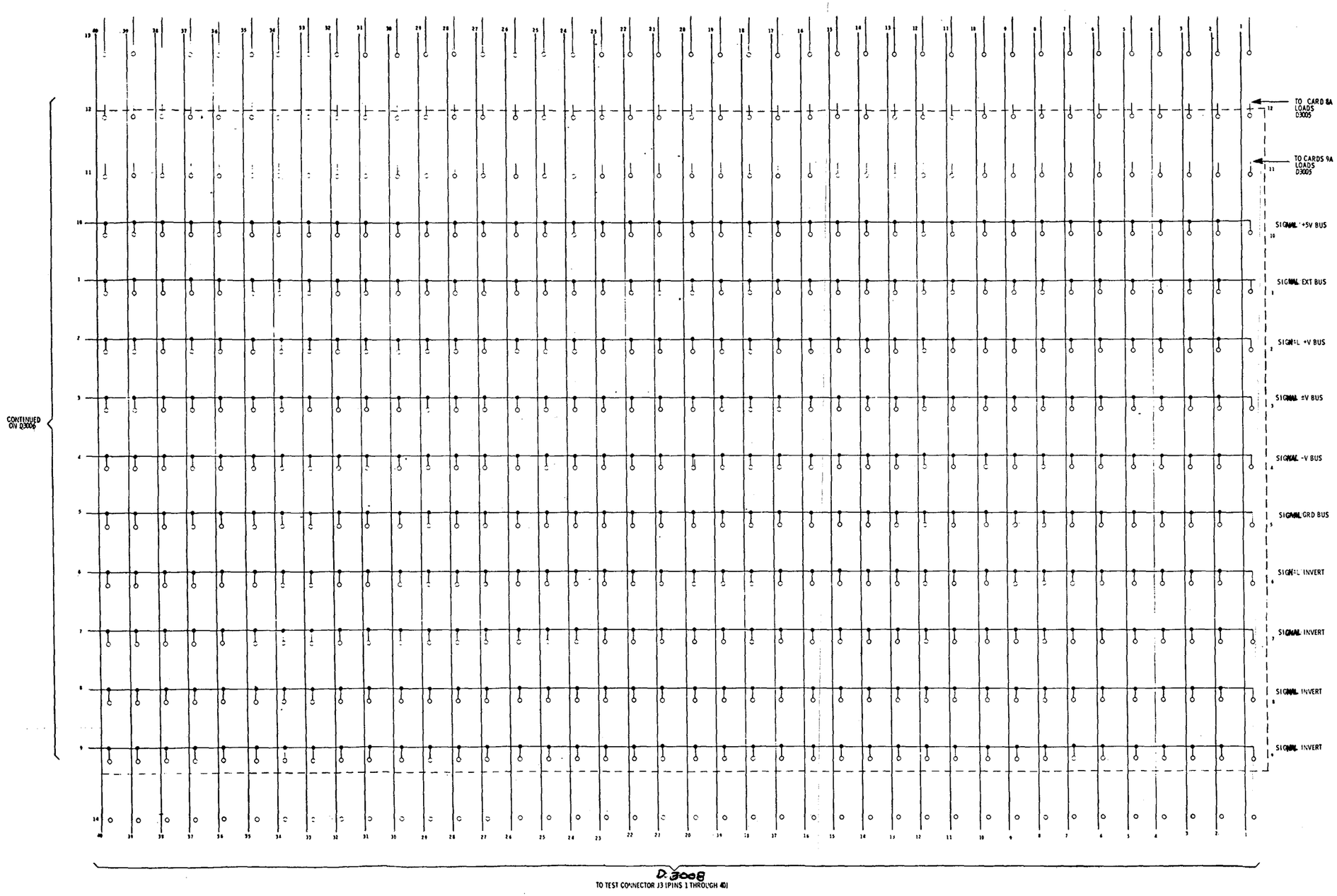
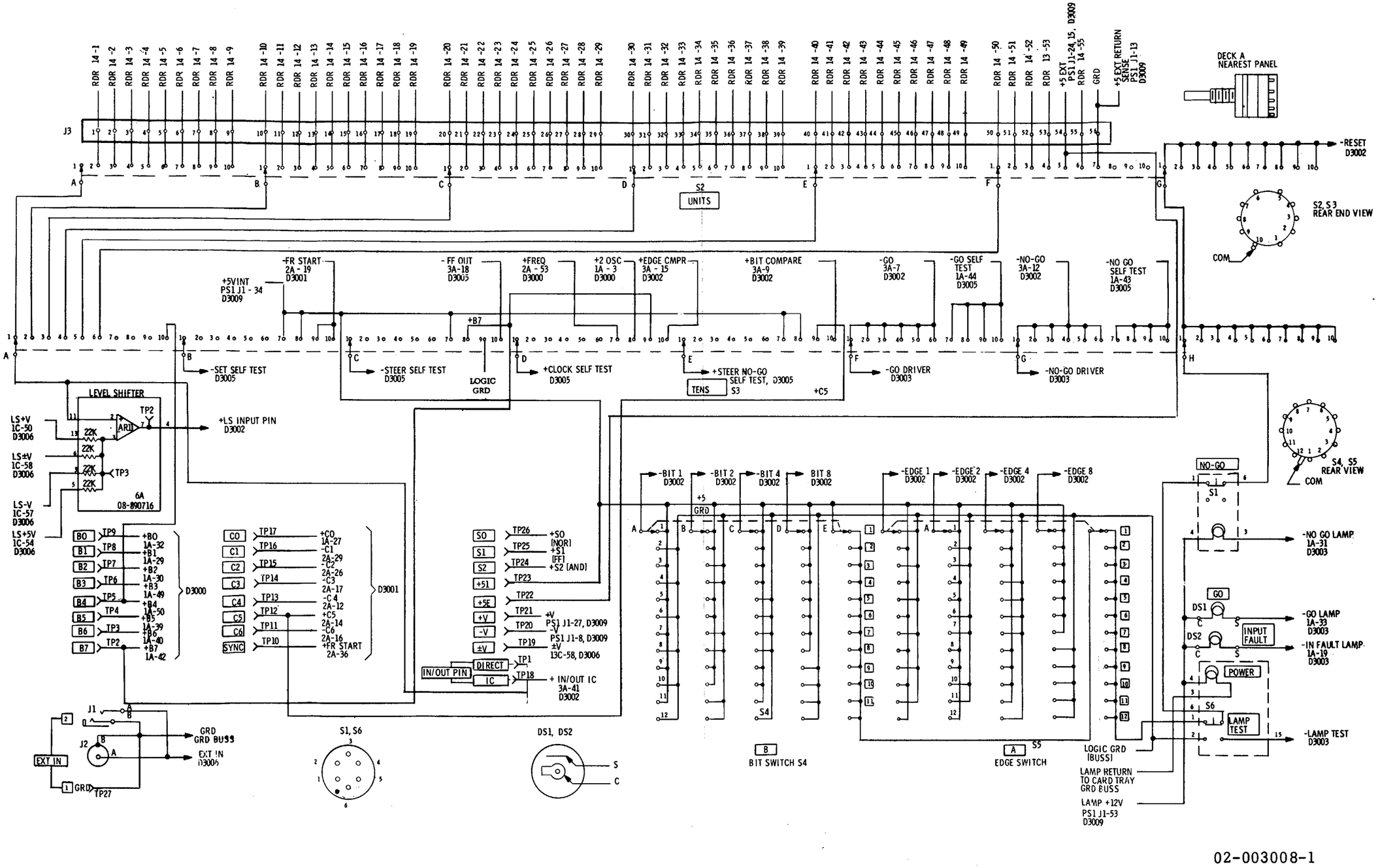


Figure 7-9 Card Reader Matrix, COL 41 through 80 Schematic Diagram



02-003007-1 O/R

Figure 7-10 Card Reader Matrix, COL 1 through 40, Schematic Diagram



02-003008-1

Figure 7-11 Card Tester Front Panel Schematic Diagram

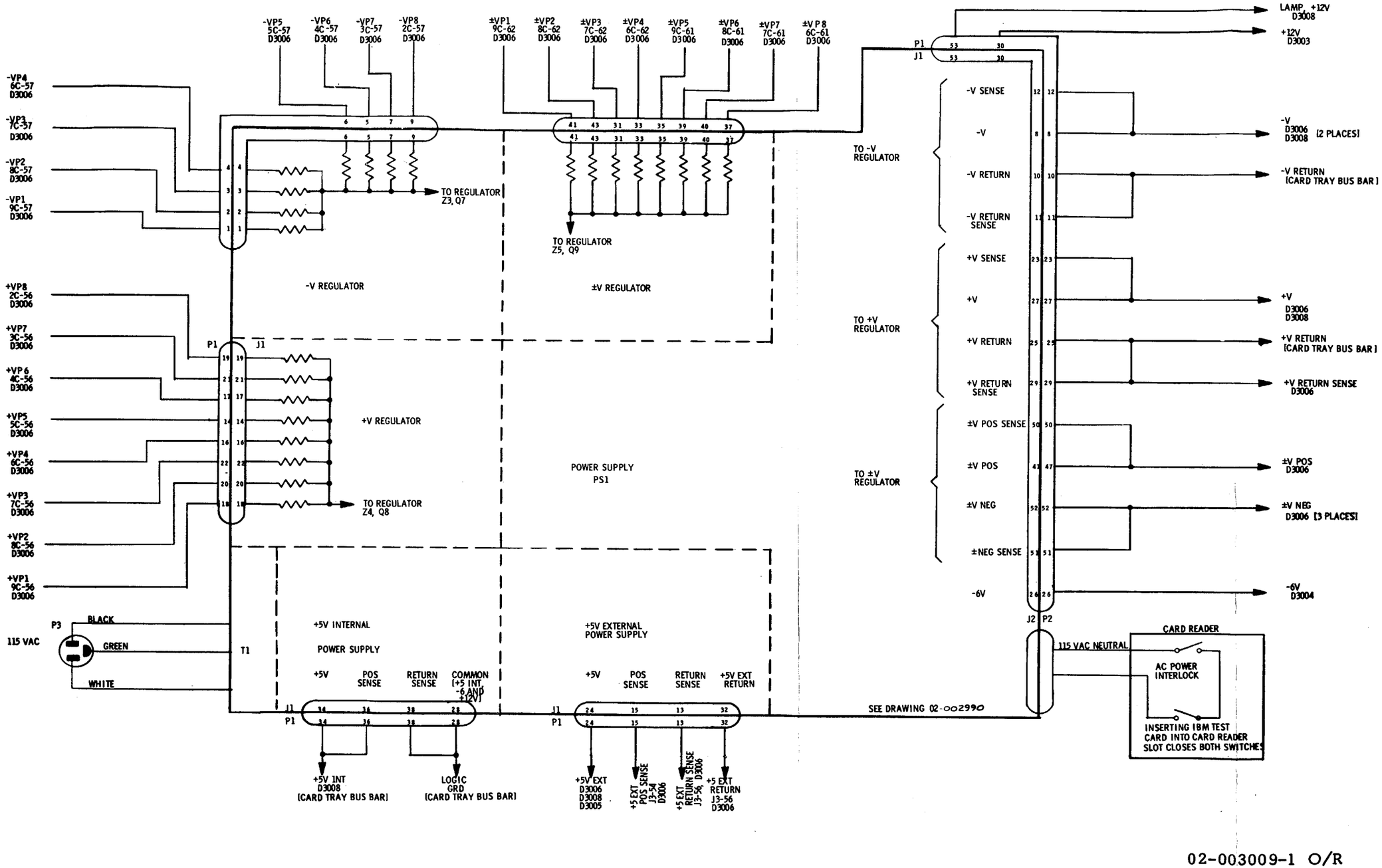


Figure 7-12 System Power Distribution, Schematic Diagram

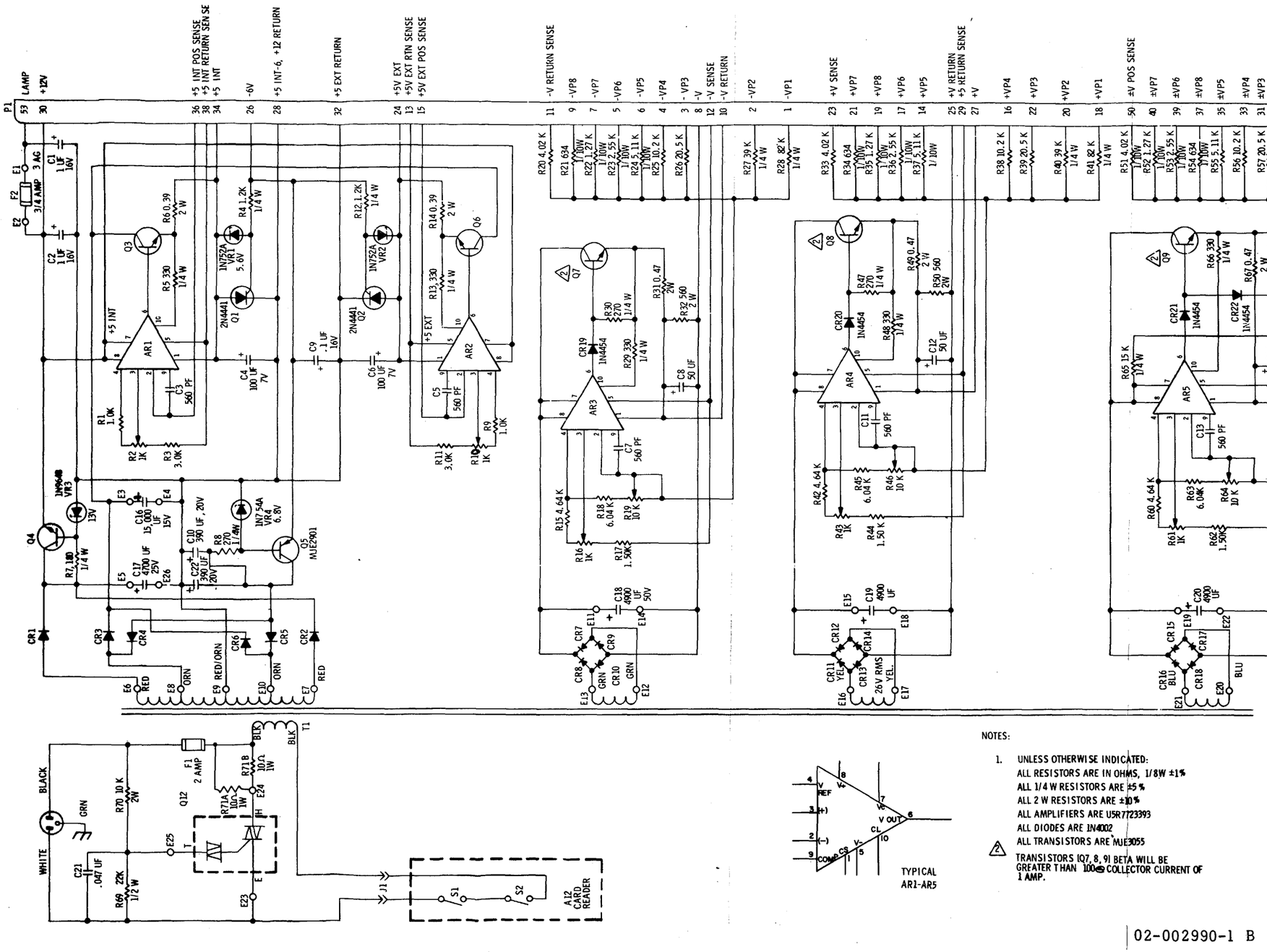


Figure 7-13 Power Supply, Schematic Diagram
7-27/7-28

SECTION VIII
PRINTED CIRCUIT CARDS.

8-1 INTRODUCTION.

This section provides maintenance information on the printed circuit cards used in the Card Tester. The information on each card includes its description, operation, logic symbols, and electrical schematic/logic diagram, mechanical configuration and parts data. Card testing information is located in section IX.

8-1.1 CARD TYPE NUMBERING. Each type of printed circuit card is identified by a Dynatronics-assigned drawing number such as 08-890710-1. This number appears on the physical card according to one of the following two conventions: (1) on digital type cards that use the test point block, the drawing number is stamped on the test point block; and, (2) on discrete component cards that do not use the test point block, the drawing number is etched on the printed circuit board itself.

On the system logic and schematic diagrams and in narrative descriptions in this manual, the type number has been shortened for convenience to the last three significant digits of the drawing number plus the "dash" number. For example, card 08-890710-1 is referred to as the 710-1 card. The "dash" number following the type number is used to indicate minor variations of the same basic card configuration such as differences in component values or deletion of a portion of the circuit on the card. In instances where the "dash"' number is omitted, the -1 configuration is implied.

8-1.2 PHYSICAL CONFIGURATION. Figure 8-1 shows a typical layout of the printed circuit cards used in the system. The card dimensions are 3°5 by 5-inches, excluding the card-edge connector area. The cards are constructed of 2-sided 1/16-inch thick G-10 epoxy with 2-ounce copper laminate with all conductor feed-through eyelets completely plated through. A 56-contact card-edge connector is used with pin numbering as shown in figure 8-1; even numbered pins are located on the component side of the card and odd-numbered pins are on the reverse side. Each card type is keyed by slots cut in the connector edge to prevent insertion of a card in a wrong connector in the system. The digital integrated circuit cards consist primarily of integrated logic circuits. The card is laid out in a 3 x 4 pattern with 12 positions for integrated circuit packs.

These positions are labeled "A" through "M", as shown in figure 8-l,as a means of identifying the packs in the parts lists and on system logic diagrams. Test points are provided at the outputs of most of the circuits on the cards, and are available at the molded test point block, The card logic/schematic diagrams in this section of the manual and the system logic/schematic diagrams carry the appropriate designations for the circuit test points. Printed circuit card 08890713-1 and -2 do not contain a Test Point blocks

8-1.3 GENERAL SPECIFICATIONS FOR DIGITAL INTEGRATED CIRCUIT CARDS.

Listed below are the general technical characteristics applicable to the integrated circuit logic cards described in this section of the manual. Any deviation from these specifications is given in the description of the individual card type.

a. Logic family: Transistor-transistor logic (T2L).
b. Propagation delay: 13 nanoseconds typical.
c. Noise immunity: 1 volt typical.
d. Recommended supply voltage (V_{cc}): +5 volts +5%.
e. Minimum supply voltage: +4.75 volts.
f. Maximum supply voltage: +7 volts.
g. Maximum input signal voltage: +5.5 volts.

h. Signal voltage levels: Graph (figure 8-2) shows typical and worst-case signal voltages.

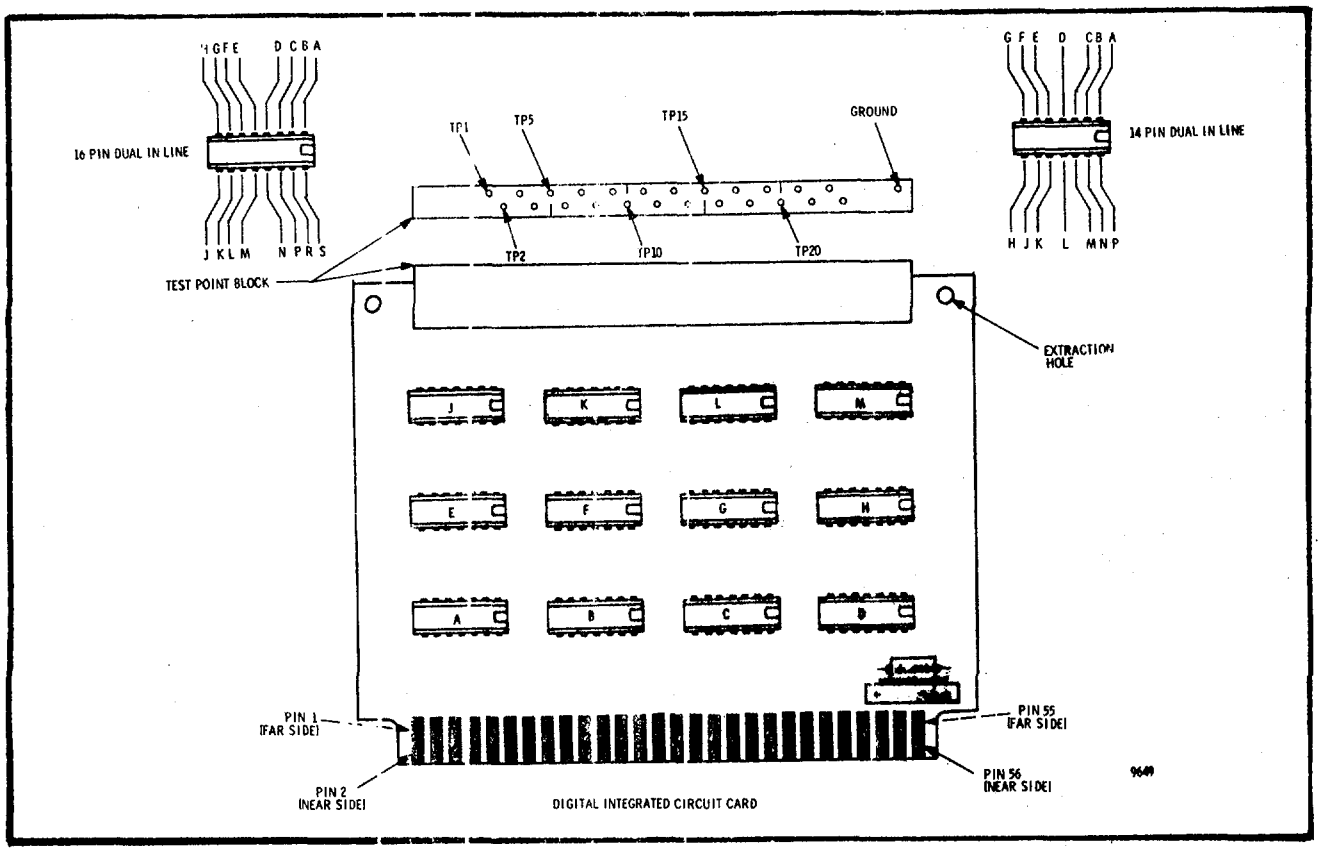


Figure 8-1. Typical Integrated Circuit Card

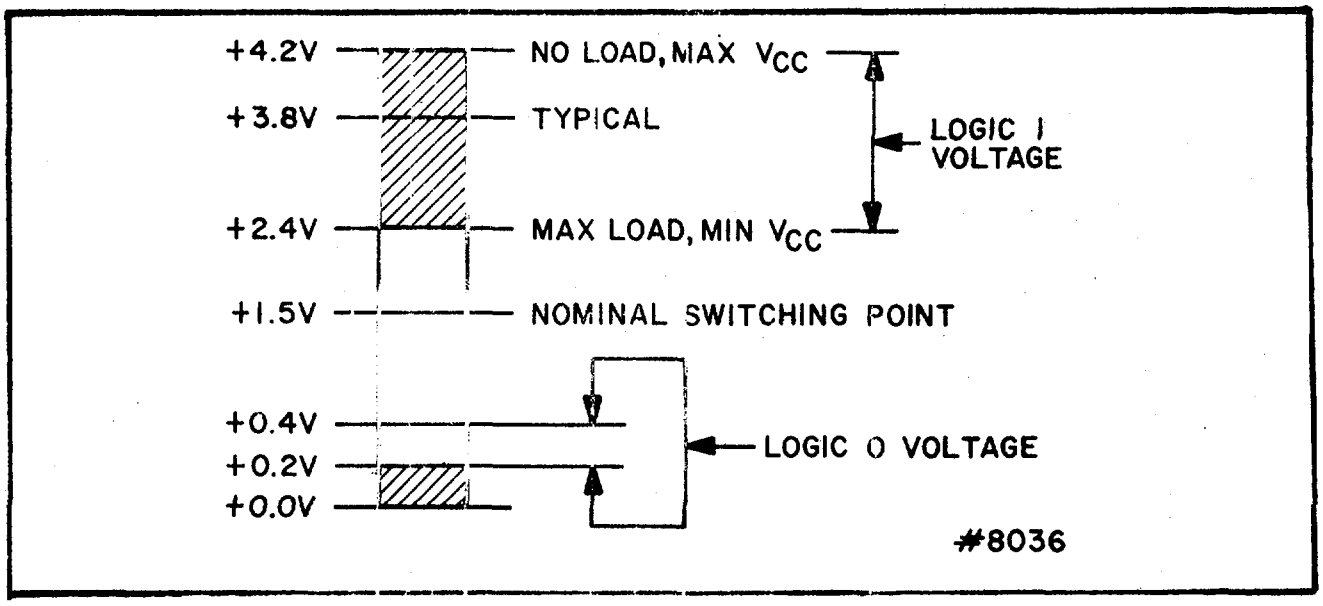


Figure 8-2. Integrated Circuit Logic Typical Signal Voltages

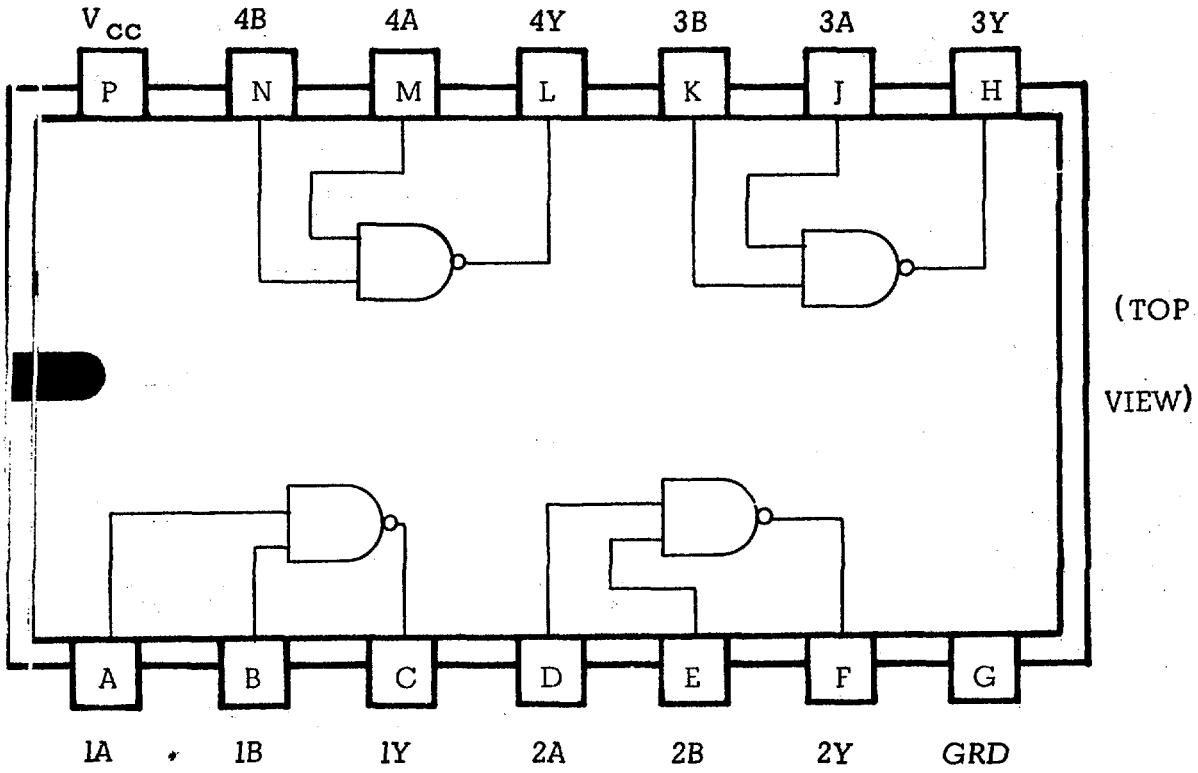
8-1.4 CARD REMOVAL AND REPLACEMENT. When removing a card from its connector, it is recommended that system power be removed first. Withdraw the card by gripping it on the top edge and rocking it back and forth until it is free. When replacing a card ensure that it is the proper type for the connector location and press it firmly into place until fully seated.

8-1.5 PRINTED CIRCUIT CARD TESTING. Test information for the Model ICT 102 Card Tester printed circuit cards is located in section IX of this manual. Paragraph 3-4 provides the basic testing procedure required by the operator of the Card Tester to check printed circuit cards.

8-1.6 INTEGRATED CIRCUIT TECHNICAL CHARACTERISTICS. The following paragraphs provide detailed characteristics of the integrated circuits contained on the printed circuit boards used in the Card Tester. The fifteen different types of integrated circuits used throughout the Card Tester are described as listed below:

a. SN7400N - Quadruple 2-Input Positive NAND Gate
b. SN7402N - Quadruple 2-Input Positive NOR Gate
c. SN7404N - Hex Inverter
d. SN7408N - Quadruple 2-Input Positive AND Gate
e. SN7410N - Triple 3-Input Positive NAND Gate
f. SN7430N - 8-Input Positive NAND Gate
g. SN7444 - Excess 3 Gray-to-Decimal Decoder
h. SN7450N - Expandable Dual 2-Wide 2-Input AND/OR/INVERT Gate
i. SN7454N - 4-Wide 2-Input AND/OR/INVERT Gates
j. SN7474N - Dual "D" Type Edge-Triggered Flip-flop
k. SN7486N - Quadruple 2-Input Exclusive OR Gate
1. SN7493N - 4-Bit Binary Counter
m. SN7495N - 4-Bit Right-Shift Left-Shift Register
n. 74H21 - High Speed Dual 4-Input AND Gate
o. SN75450N - Multi-Purpose Interface Circuit

8-1.6.1 Integrated Circuit SN7400N Quadruple 2-Input Positive NAND Gate.



TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7400'N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated circuits delineated in paragraph 8-1,3.

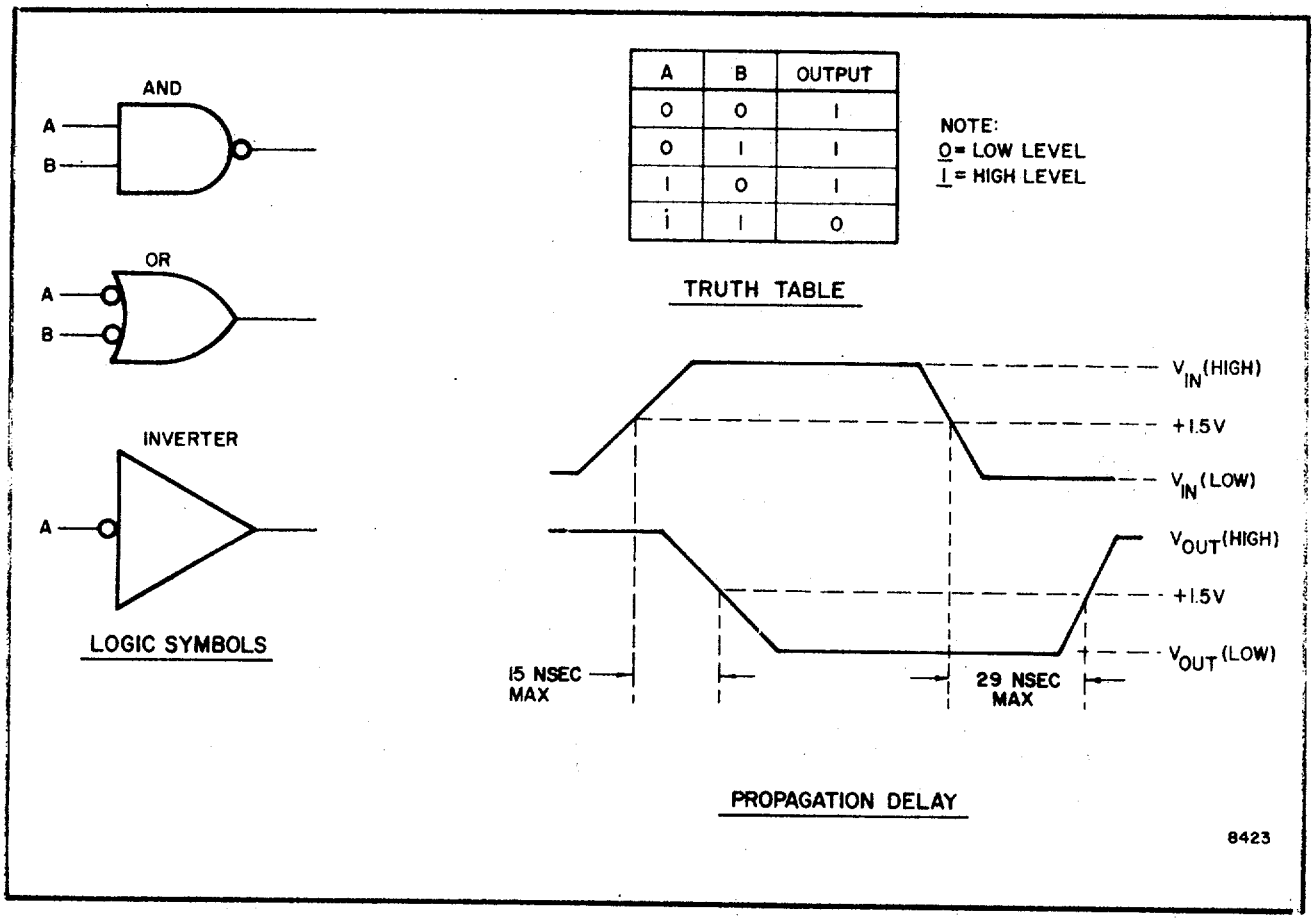
a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive with respect to ground.

c. Output Current: Maximum capability is to accept 16 milliamperes (current: sink) when the output is at a low level and to supply 9.1 milliamperes (current: source) when the output is at a high level.

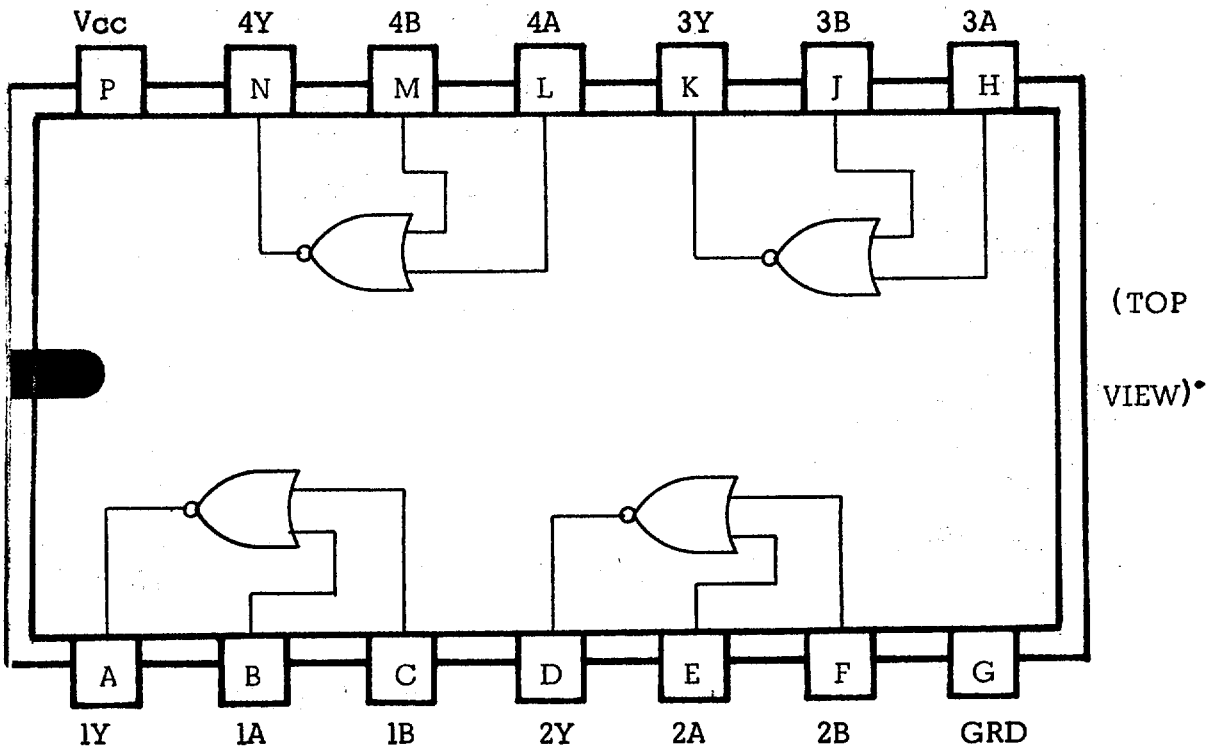
d. No more than one gate output in each pack should be shorted to ground at the same time.

e. Supply Voltage (V_{CC}): Should be +5.0 volts $\pm$5%.



Two-Input Nand Gate Logic Symbols, Truth Table and Propagation Delay

8-1.6.2 Integrated Circuit SN7402N Quadruple 2-Input Positive NAND Gate.



TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN740'N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated·circuits delineated in paragraph 8-1.3.

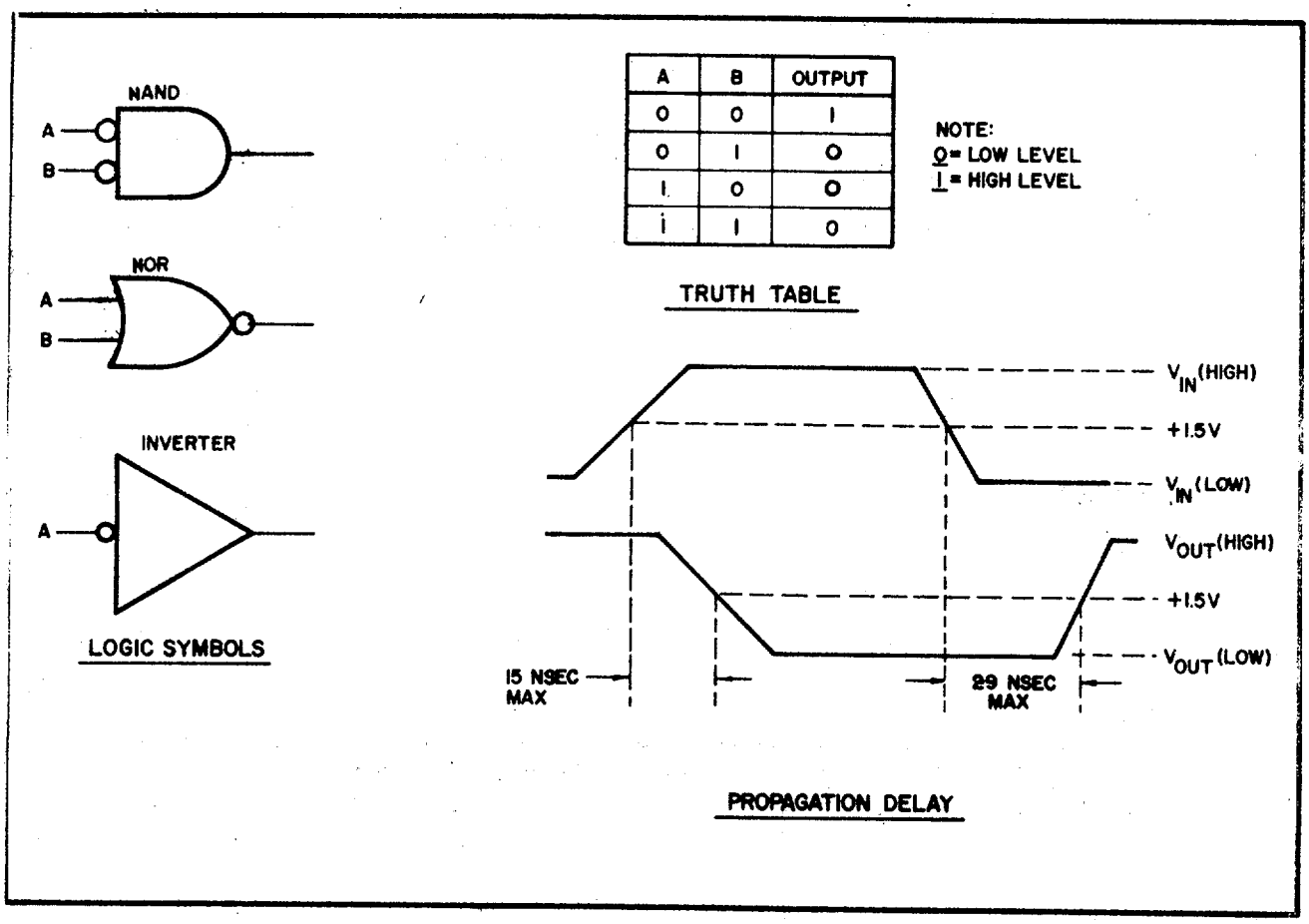
a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive with respect to ground.

c. Output Current: Maximum capability is to accept 16 milliamperes (current link) when the output is at a low level and to supply 9.1 milliamperes (current source) when the output is at a high level.

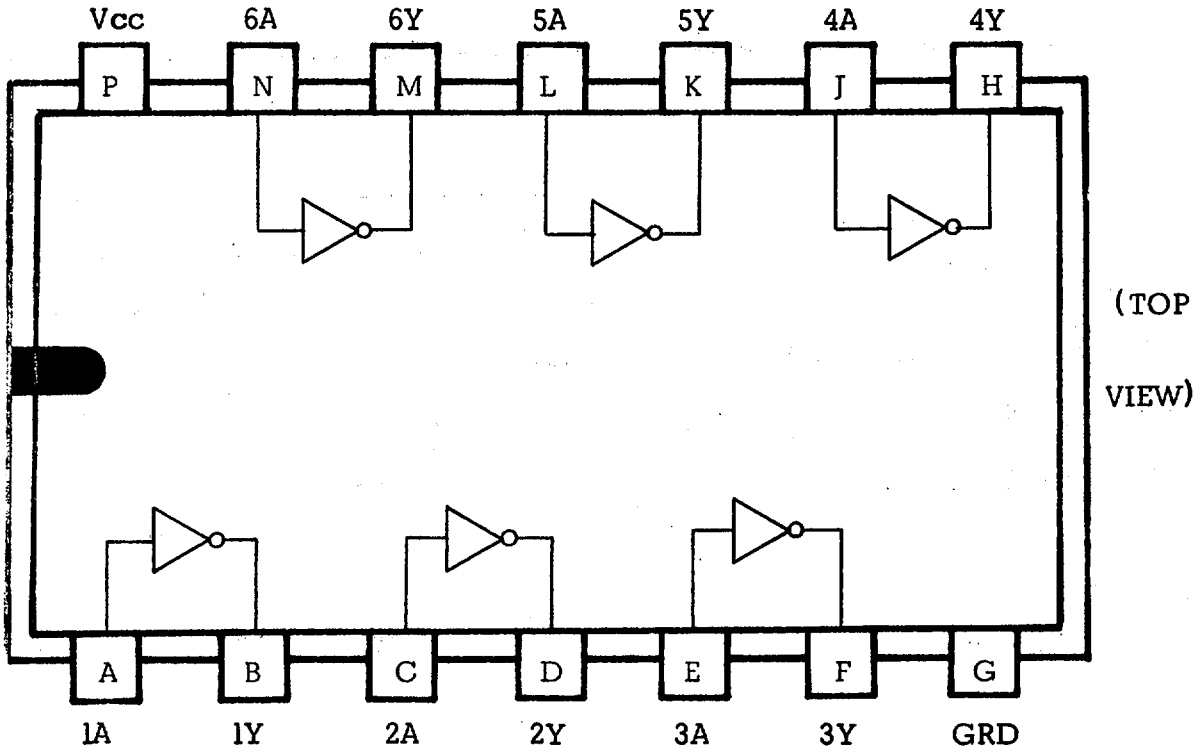
d. No more than one gate output in each pack should be shorted to ground at the same time.

e. Supply Voltage (V_{CC}): Should be +5.0 volts ±5% .



Two-Input NOR Gate Logic Symbols, Truth Table and Propagation Delay

8-1.6.3 Integrated Circuit SN7404N Hex Inverter.



TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7404N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated circuits delineated in paragraph 8-1.3.

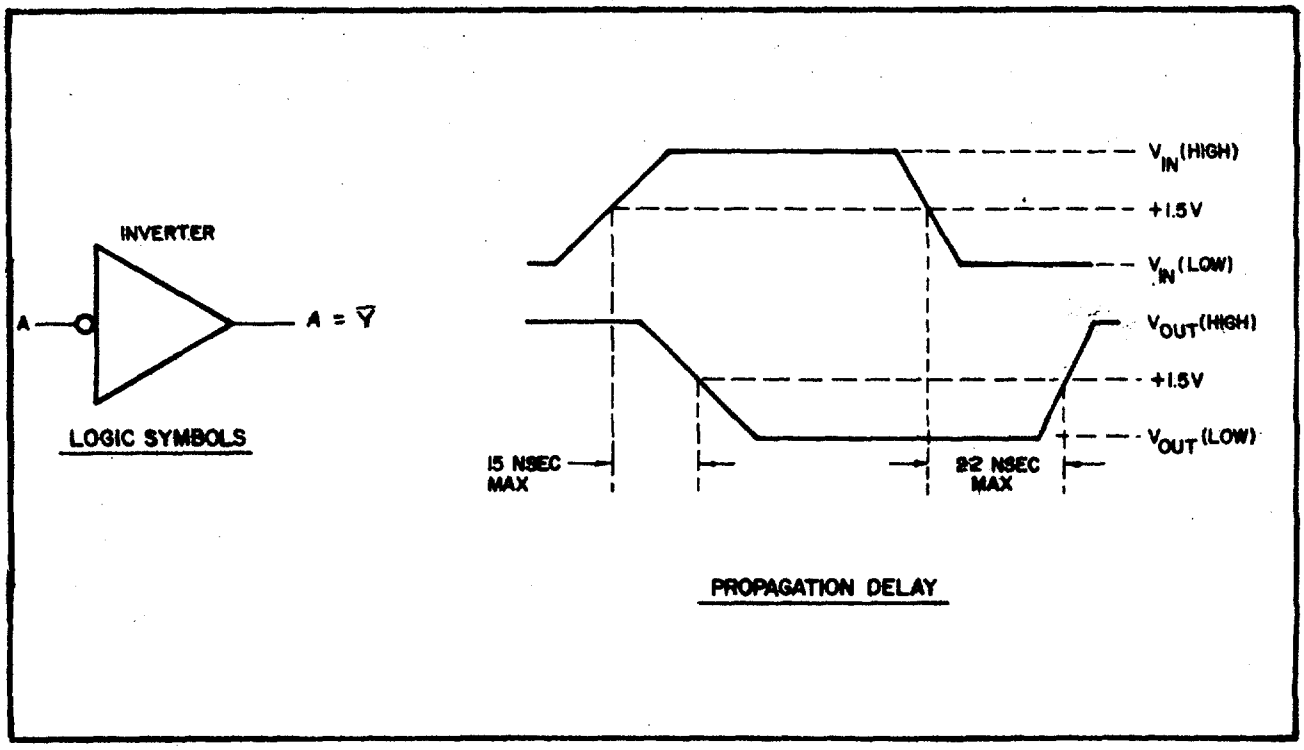
a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive with respect to ground.

c. Output Current: Maximum capability is to accept 16 milliamperes (current 'Sink) when the output is at a low level and to supply 9.1 milliamperes (current source) when the output is at a high level.

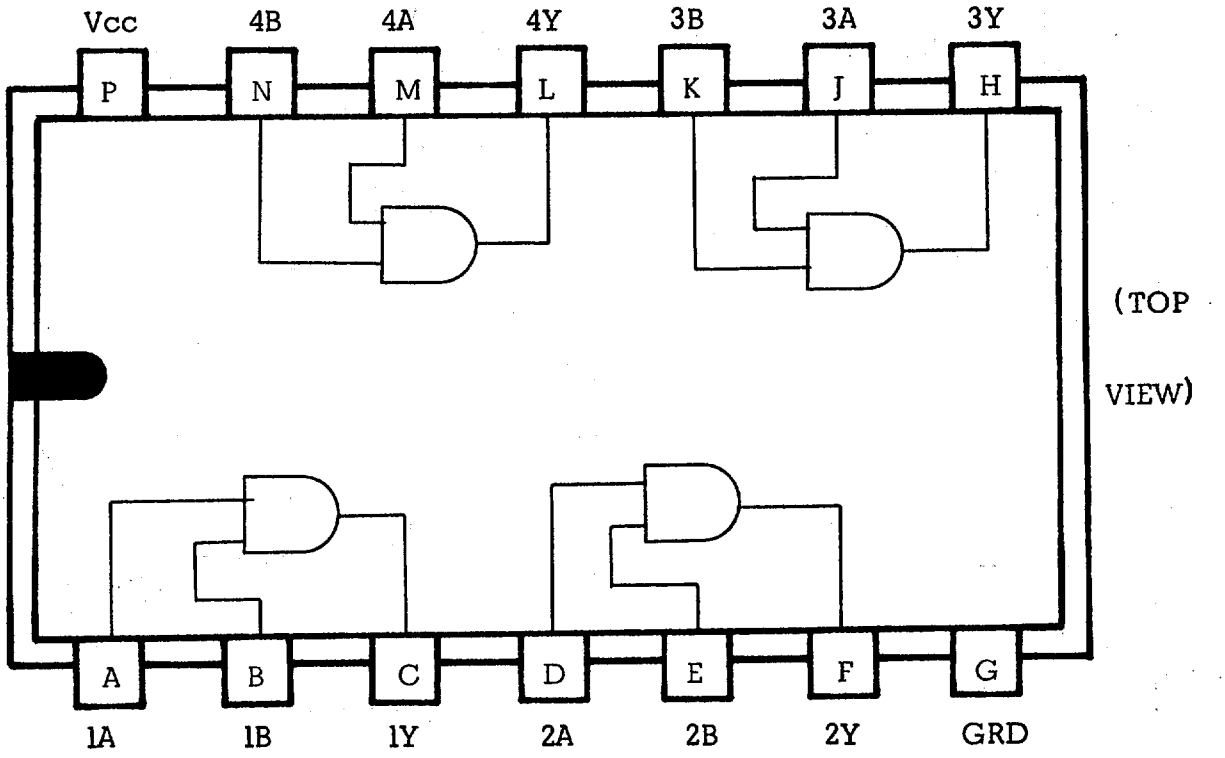
d. No more than one inverter output in each pack should be shorted to ground at the same time.

e. Supply Voltage (V_{cc}):. Should be +5.0 volts ±5%.



Hex Inverter Logic Symbols, and Propagation Delay

8-1.6.4 Integrated Circuit SN7408N Quadruple 2-Input Positive AND Gate.



TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7408N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated circuits delineated in paragraph 8-1.3.

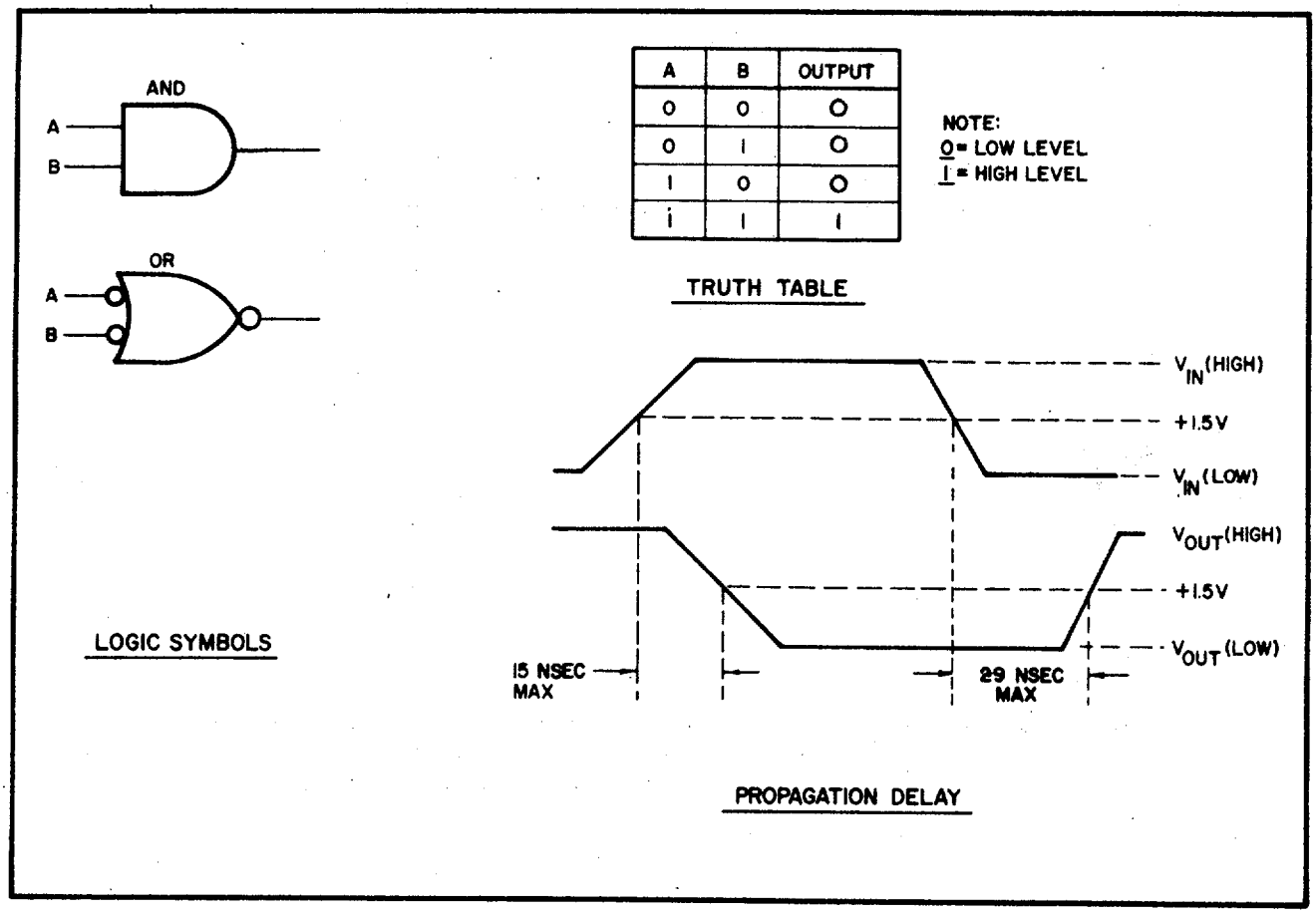
a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive-with respect to ground.

c. Output Current: Maximum capability is to accept 16 milliamperes (current sink) when the output is at a low level and to supply 9.1 milliamperes (current source) when the output is at a high level.

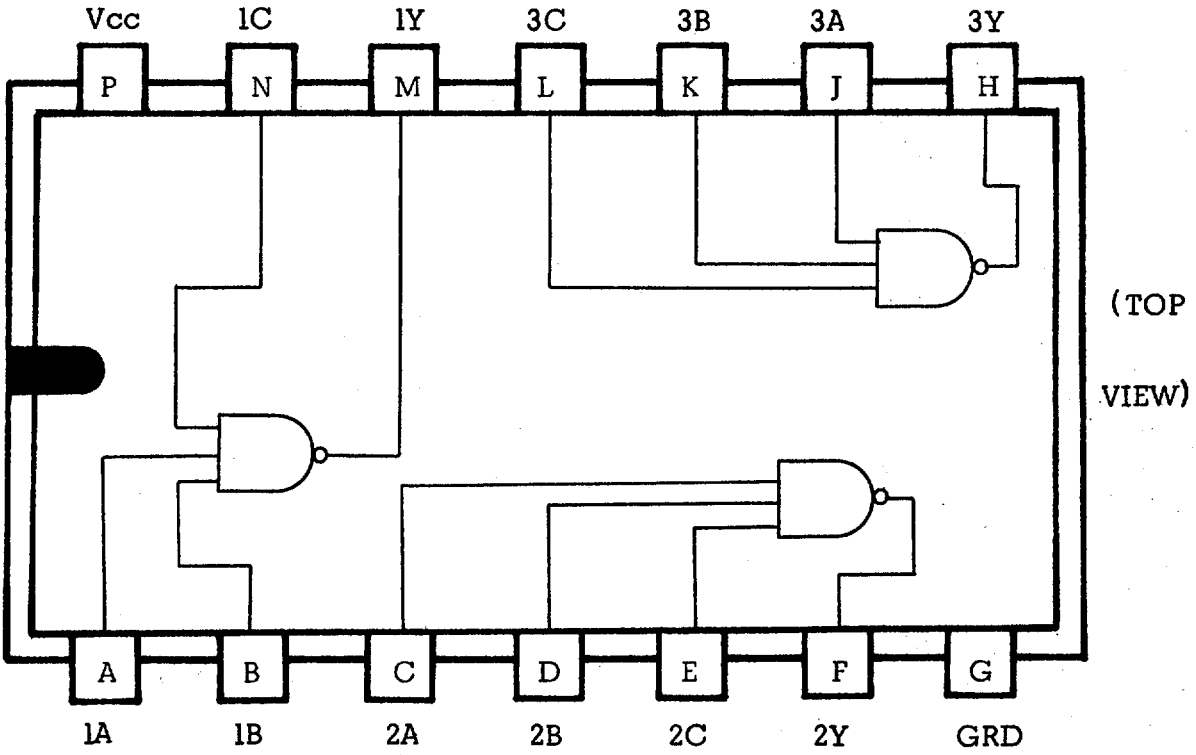
d. No more than one gate output in each pack should be shorted to ground at the same time.

e. Supply Voltage (V_{CC}): Should be +5.0 volts ±5%.



Two-Input AND Gate Logic Symbols, Truth Table and Propagation Delay

8-1.6.5 Integrated Circuit SN7410N Triple 3-Input Positive NAND Gate.



TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7410N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated circuit delineated in paragraph 8-1.3.

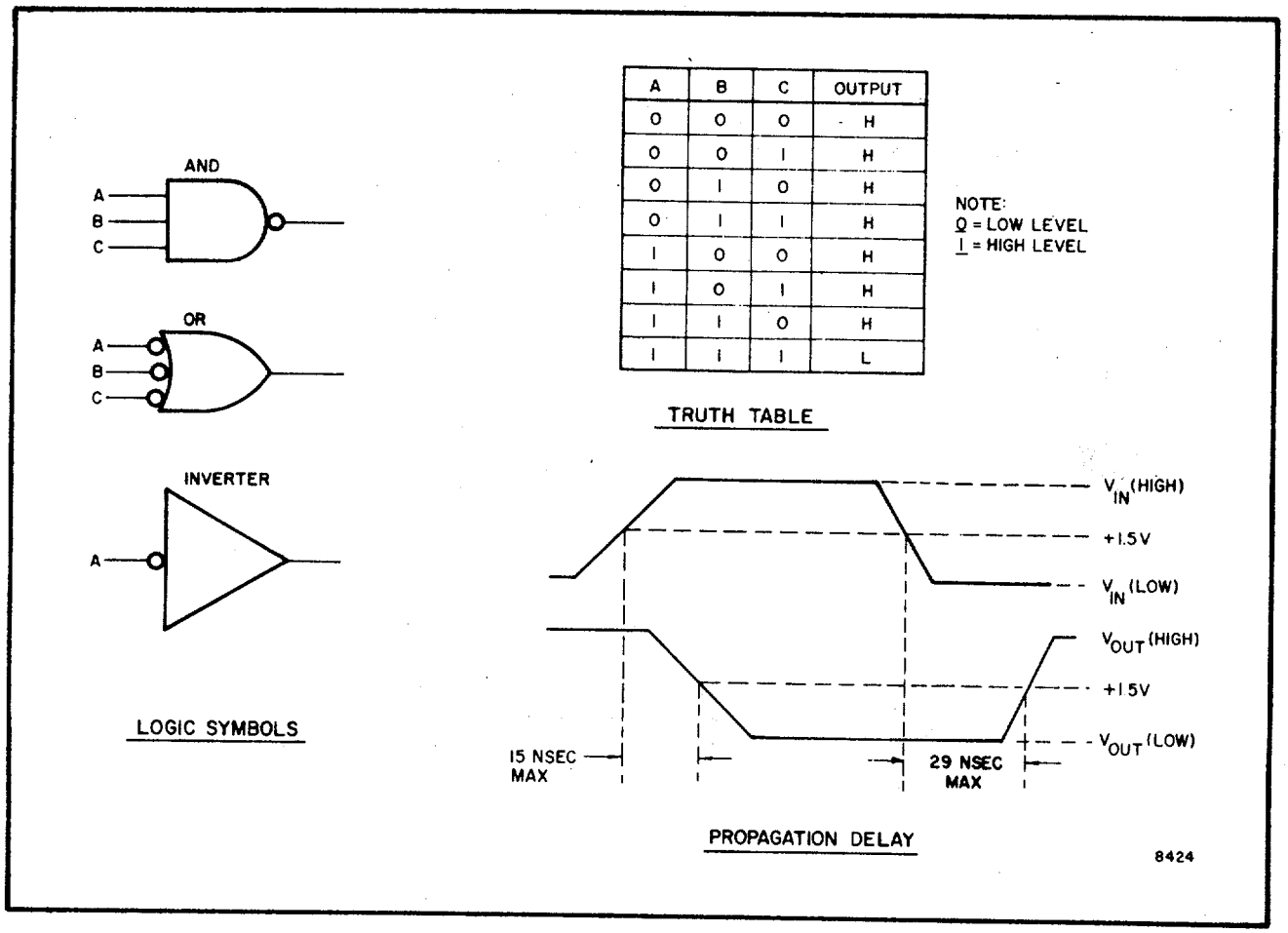
a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive with respect to ground.

c. Output Current: Maximum capability is to accept 16 milliamperes (current sink) when the output is at a low level and to supply 9.1 milliamperes (current source) when the output is at a high level.

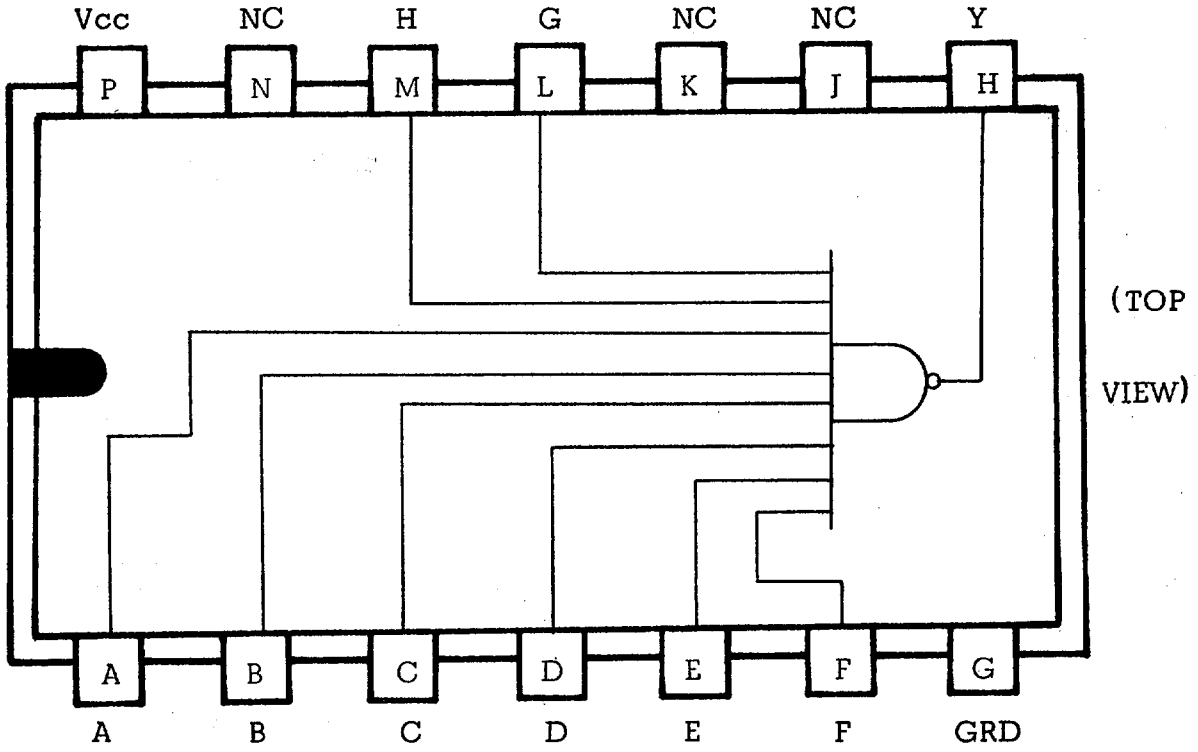
d. No more than one gate output in each pack should be shorted to ground at the same time.

e. Supply Voltage (V_{CC}): Should be +5.0 volts ±5%.



Three-Input Nand Gate Logic Symbols, Truth Table, and Propagation Delay

8-1.6.6 Integrated Circuit SN7430N 8-Input Positive NAND Gate.



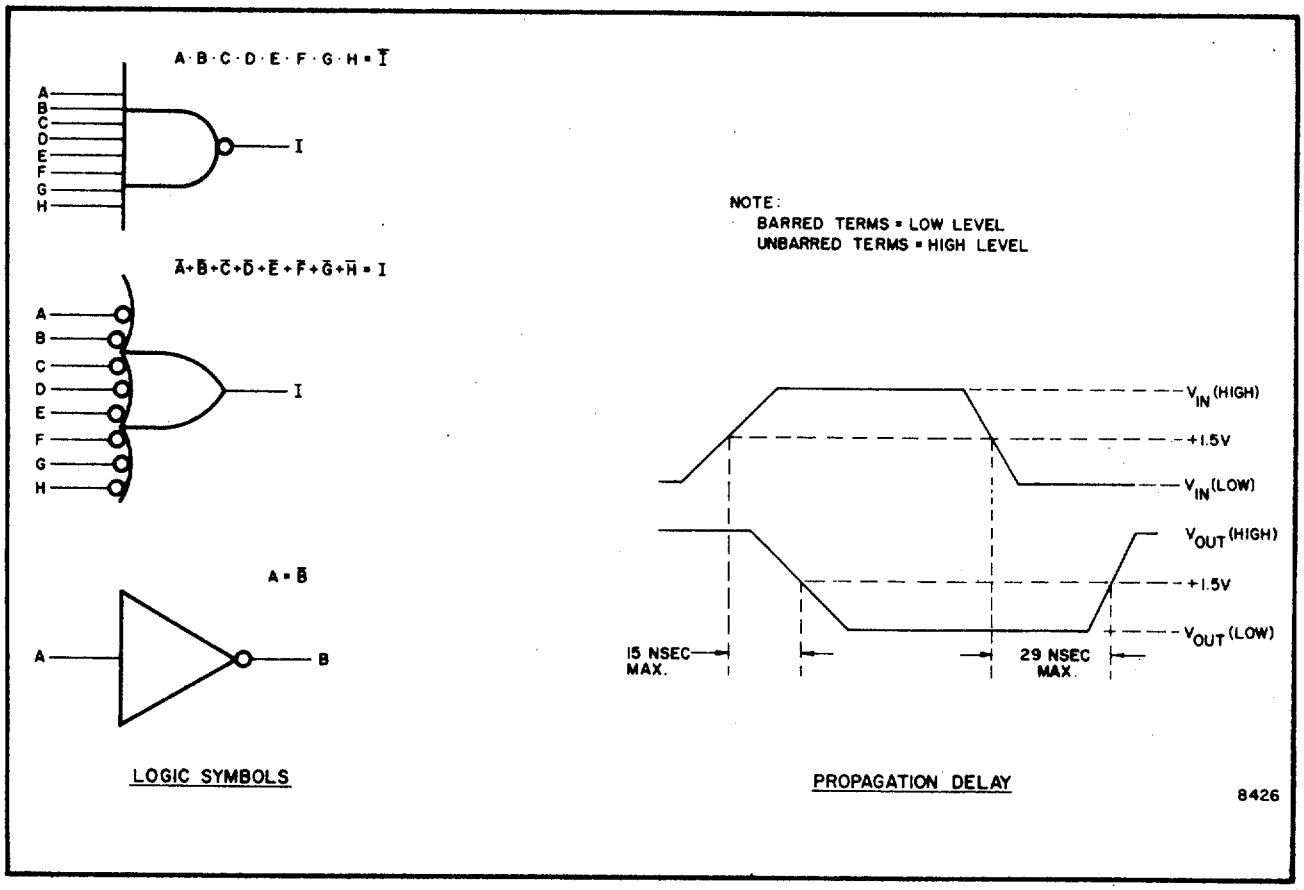
TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7430N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated circuits delineated in paragraph 8-1.3.

a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive with respect to ground.

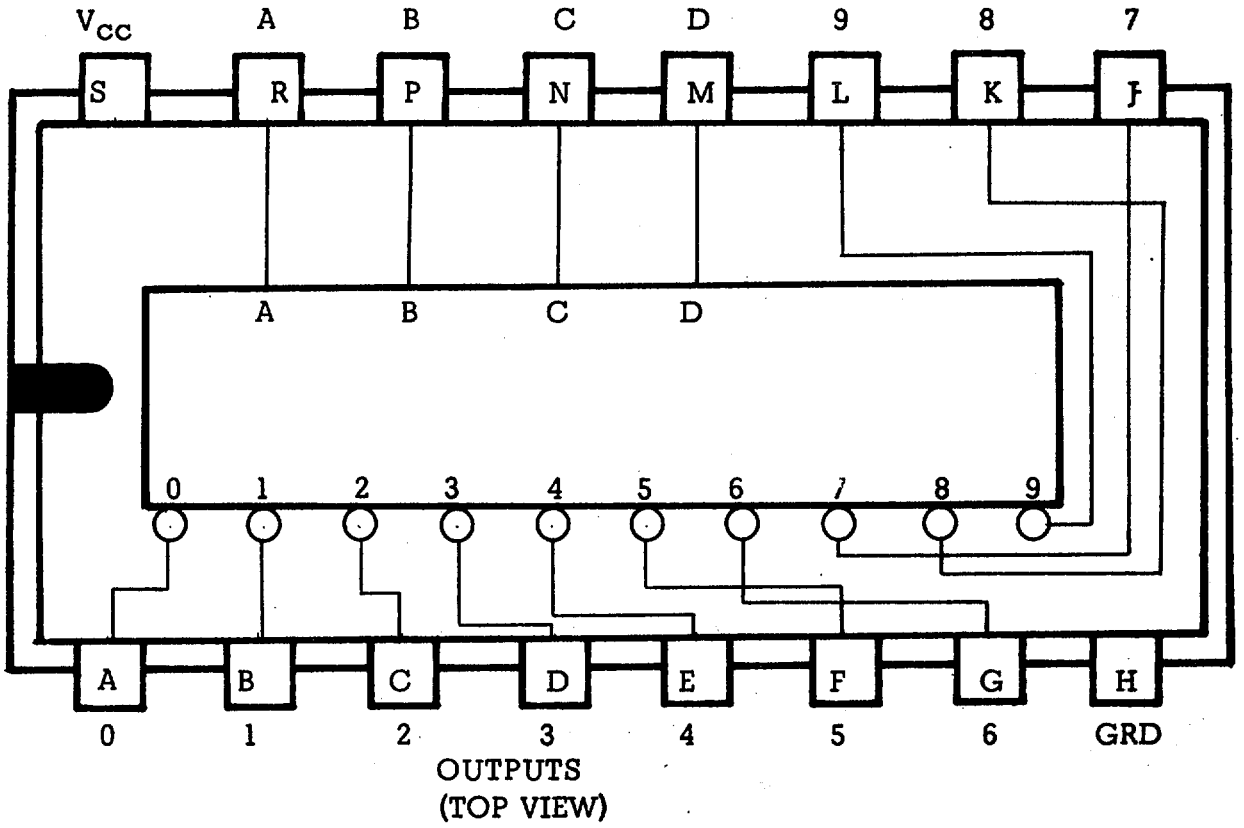
c. Output Current: Maximum capability is to accept 16 milliamperes (current sink) when the output is at a low level and to supply 9.1 milliamperes (current source) when the output is at a high level.

d. Supply Voltage (V c): Should be +5.0 volts +5%.



Eight-Input Nand Gate Logic Symbols and Propagation Delay

8-1.6.7 Integrated Circuit SN7444N Excess 3 Gray-to-Decimal Decoder.



NOTE:
1. Logic 1 = High level
2. Logic 0 = Low level

TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7444N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated circuits delineated in paragraph 8-1.3.

a. Input Signal Voltage: Must not exceed +5.5 volts.

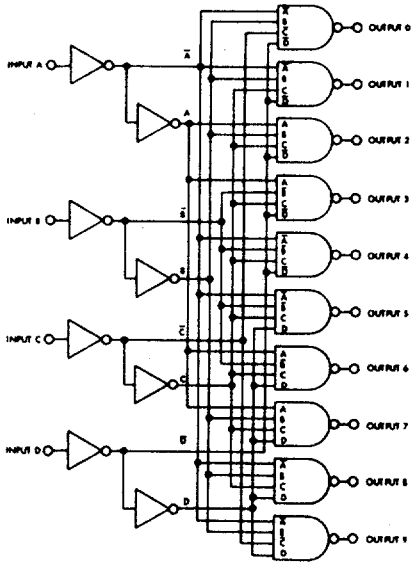
b. Input Signal Polarity: Must be positive with respect to ground.

c. Output Current: Maximum capability is to accept 16 milliamperes (current sink) when the output is at a low level and to supply 9.1 milliamperes

(current source) when the output is at a high level.

d. Supply Voltage (V_{CC}): Should be +5.0 volts ±5%.

e. Equivalent Circuit

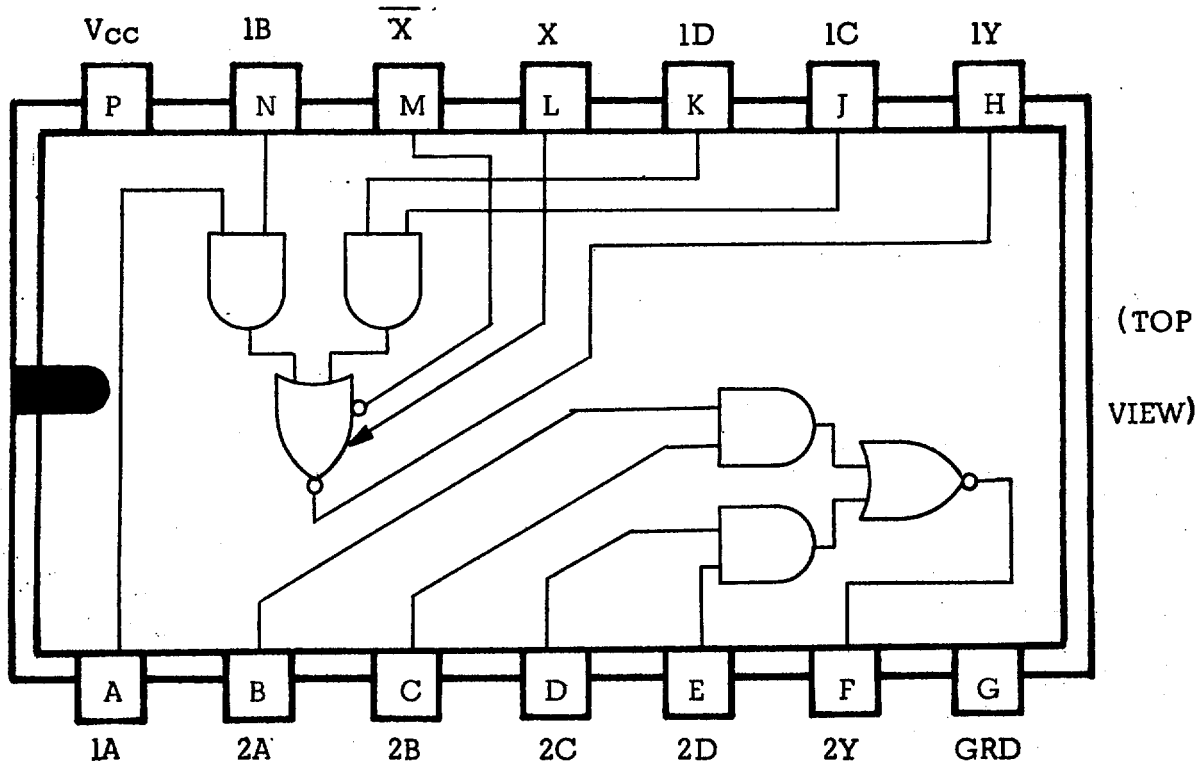


SN5444/SN7444 EXCESS-3-GRAY-TO-DECIMAL

f. Truth Table

SN5444/SN7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	1	1	1	1
1	1	0	1	1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	1	1	0	1
1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1

8-1.6.8 Integrated Circuit SN7450N 2-Wide Expandable 2-Input AND/OR/INVERT Gate.



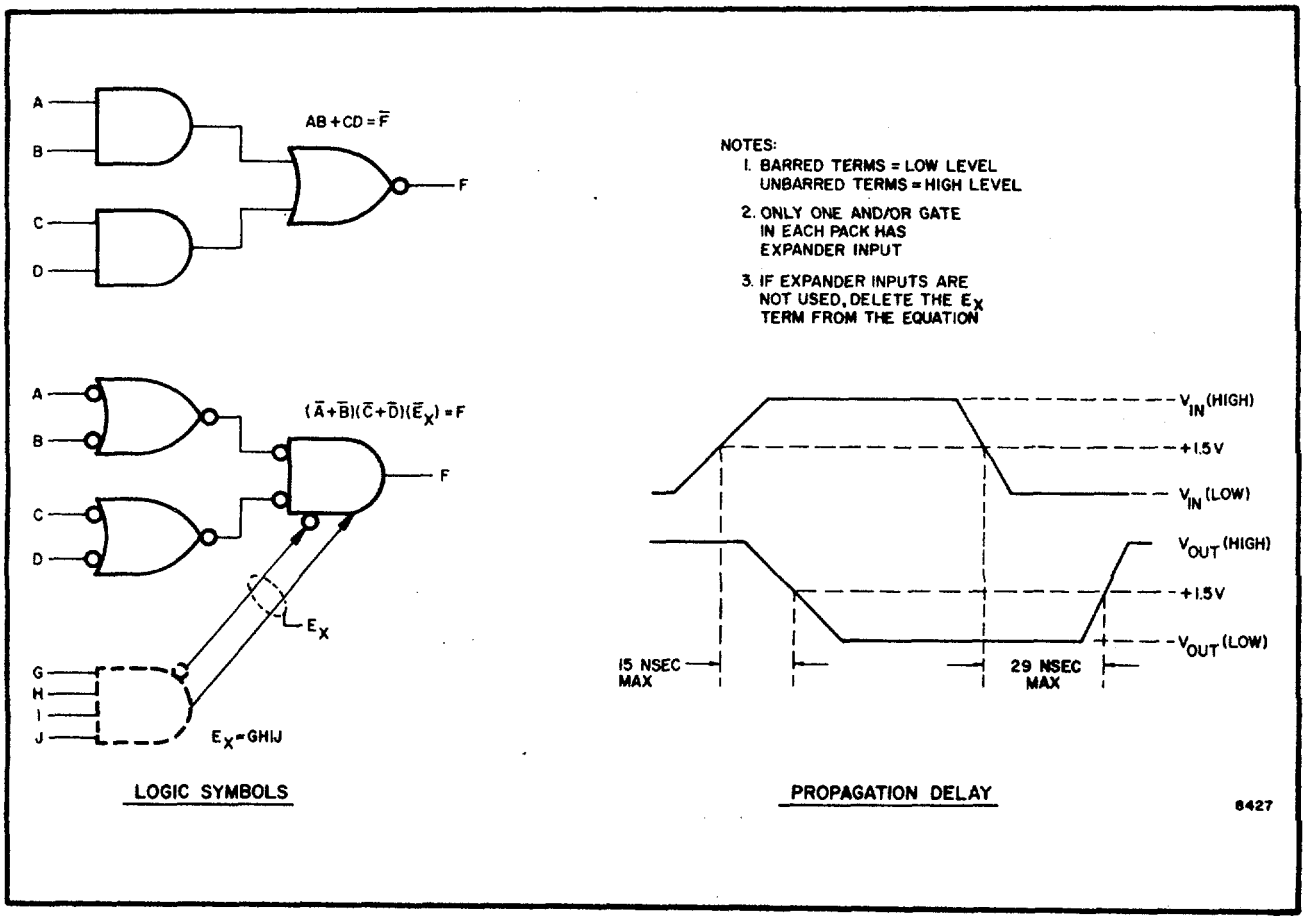
TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7450N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated circuits delineated in paragraph 8-1.3.

a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive with respect to ground.

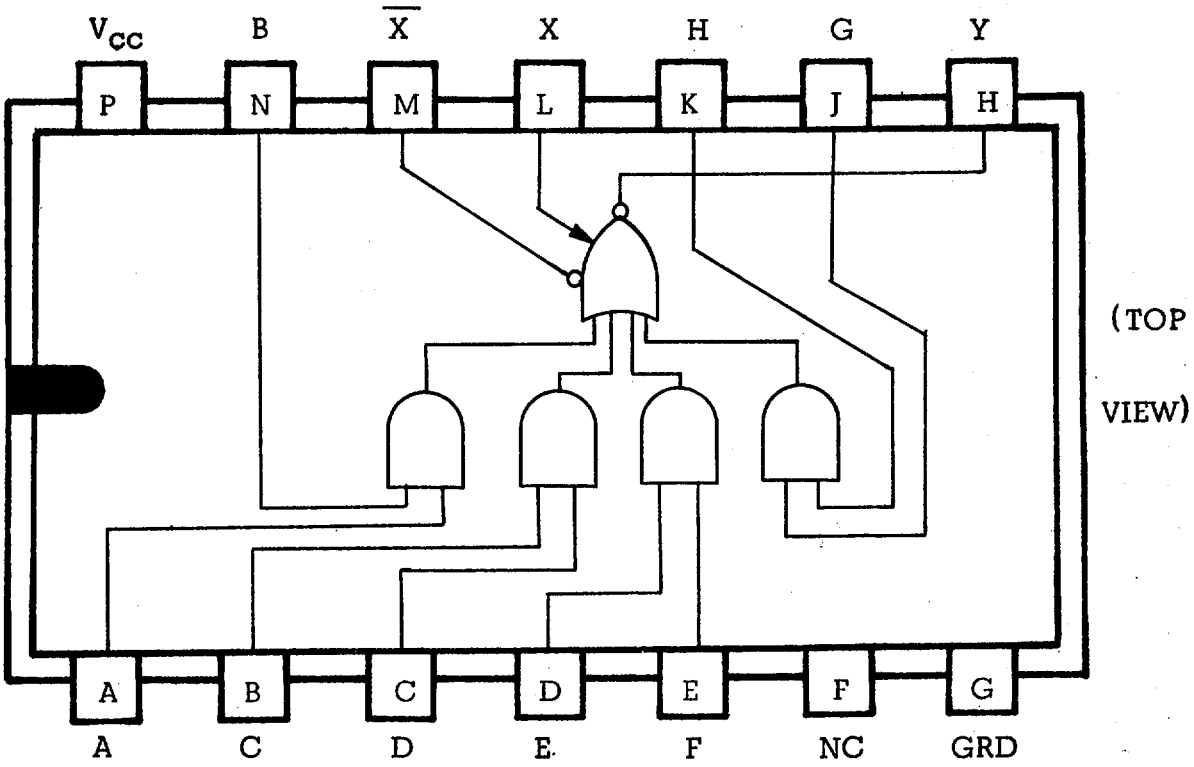
c. Output Current: Maximum capability is to accept 16 milliamperes (current sink) when the output is at a low level and to supply 9.1 milliamperes (current source) when the output is at a high level.

d. Supply Voltage (V_{CC}): Should be +5.0 volts ±5%.



Dual And/Or Gate Logic Symbols and Propagation Delay

8-1.6.9 Integrated Circuit SN7454N 4-Wide Expandable 2-Input AND/OR/INVERT Gates.



NOTE:

1. Make no external connections to X and X pins.

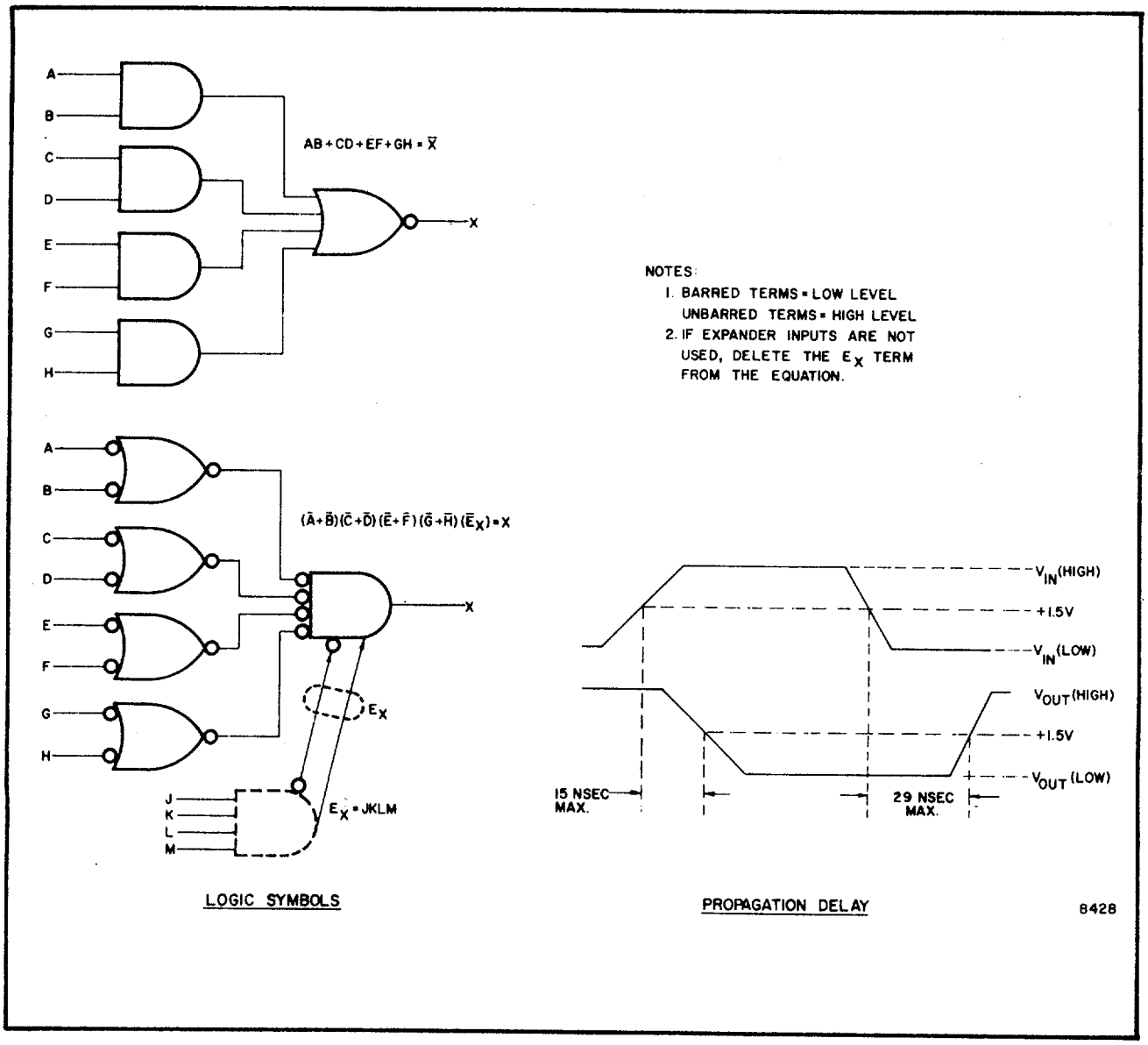
TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7454N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to. all digital integrated circuits delineated in paragraph 8-1.3.

a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive with respect to ground

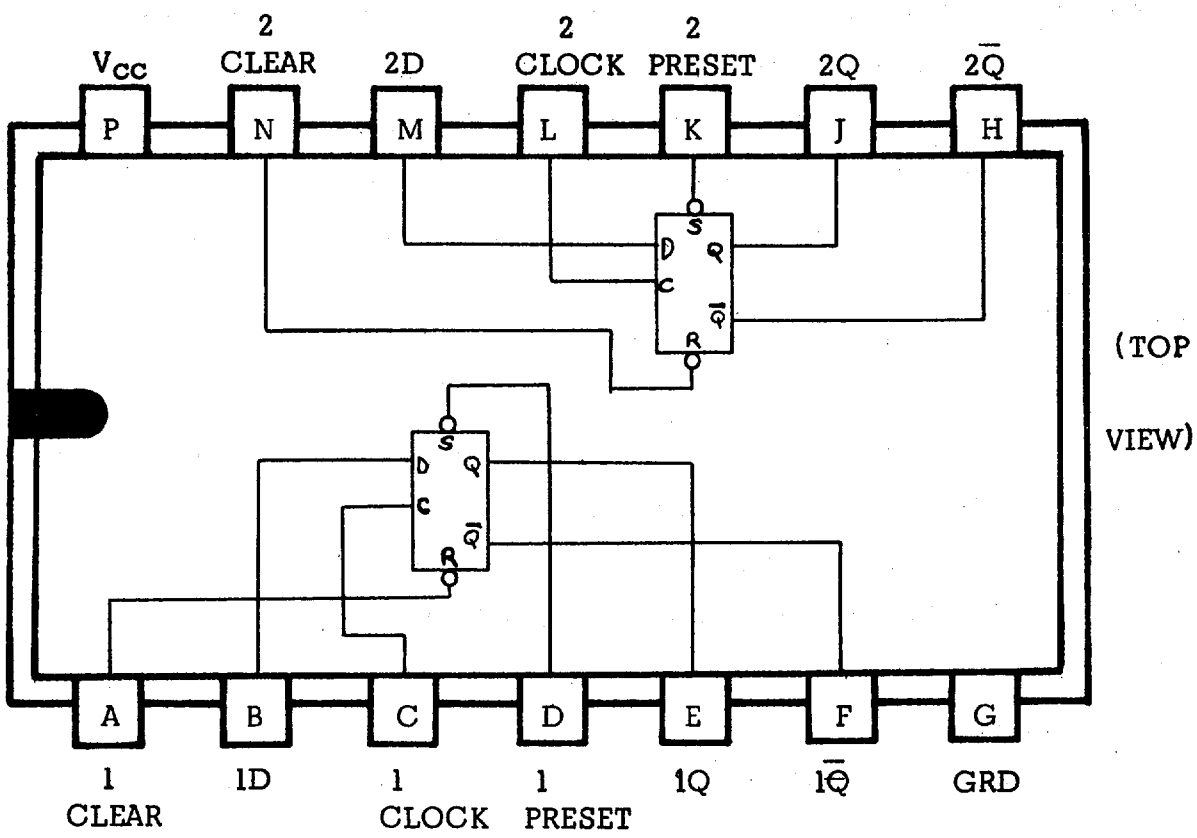
c. Output Current: Maximum capability is to accept 16 milliamperes (current sink) when the output is at a low level and to supply 9.1 milliamperes (current source) when the output is at a high level.

d. Supply Voltage (V_{CC}): Should be +5.0 volts ±5%.



Quad AND/OR Gate Logic Symbols and Propagation Delay

8-1.6.10 Integrated Circuit SN7474N Dual "D" Type Flip-flop.



TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7474N integrated circuit are given below. Refer also to the general characteristics applicable to all digital integrated circuit cards provided in paragraph 8-1.3, at the beginning of this section of the manual.

a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive with respect to ground.

c. Output Current: Maximum capability is to accept 16 milliamperes (current sink) when the output is at the low level and to supply 9.1 milliamperes (current source) when the output is at the high level.

d. No more than one output in each pack should be shorted to ground at one time.

e. Supply Voltage (V_{cc}): Should be +5.0 volts +5%.

TIMING AND OPERATING CONSIDERATIONS. As shown in the timing diagram the switching time measurements are with reference to the +1.5 volt threshold points. The level to be stored in the flip-flop must be present at the DATA input for a period of time (T_{setup}) before the CLOCK pulse crosses the threshold level and remain for a time (T_{hold}) thereafter. Propagation delay (T_{pd}) is measured from the time the CLOCK crosses the threshold to the time the OUTPUT crosses the threshold. Additional specific timing and control information is listed below:

a. Input DATA is transferred to the Q OUTPUT on the positive edge of the CLOCK pulse.

b. Clock triggering occurs at a voltage level of the CLOCK pulse and is not directly related to the transition time of the pulse.

c. Maximum toggle frequency is 15 MHz.

d. Maximum propagation delay (T_{pd}) to switch Q OUTPUT to high level is 35 nanoseconds; maximum Tpd to switch Q OUTPUT to low level is 50 nanoseconds.

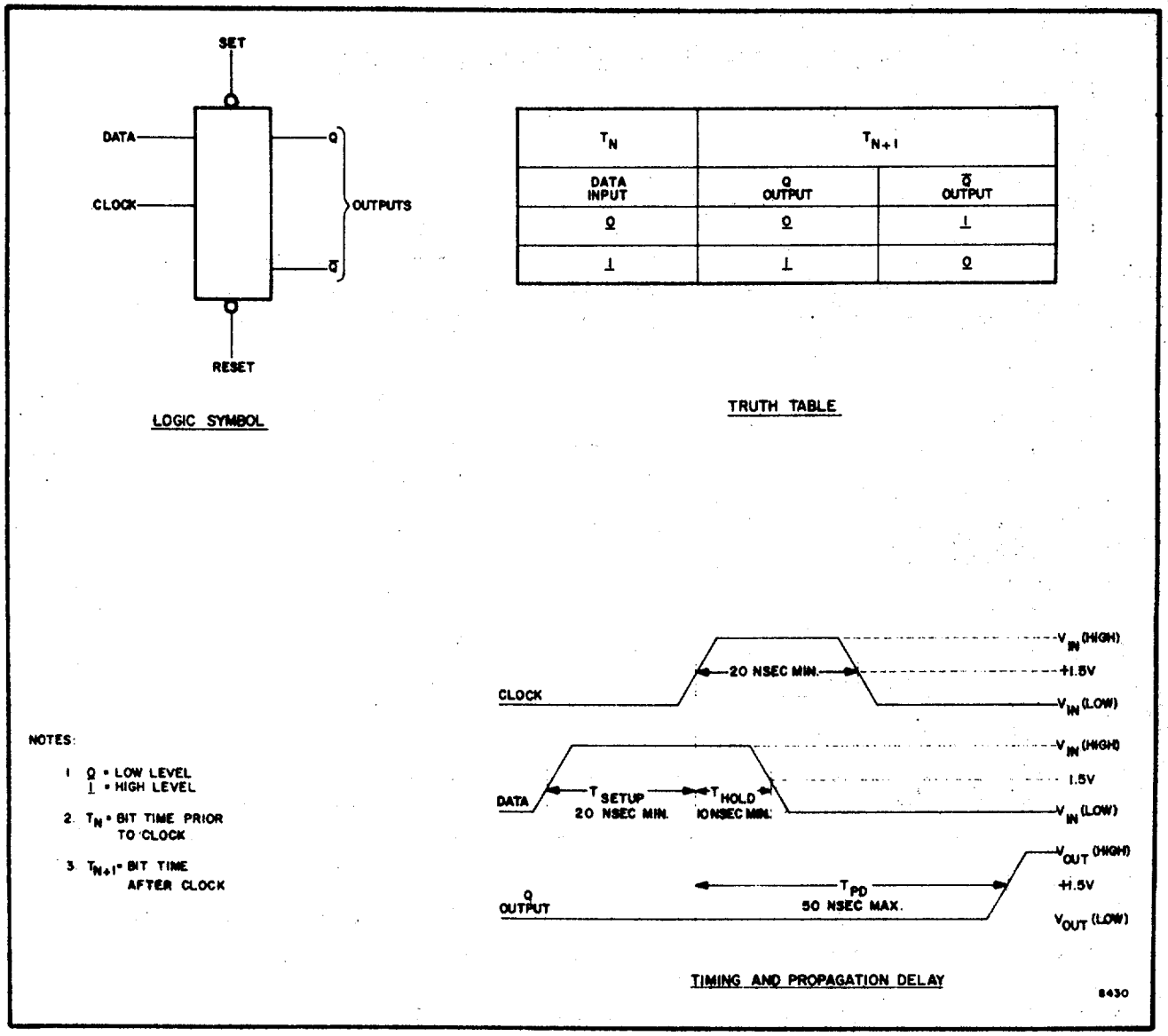
e. Low levels to the SET or RESET inputs take priority over the CLOCK and DATA inputs.

f. The $\overline{Q}$ and Q outputs are complementary.

g. Low level to SET input forces the $\overline{Q}$ OUTPUT to L,, high level.

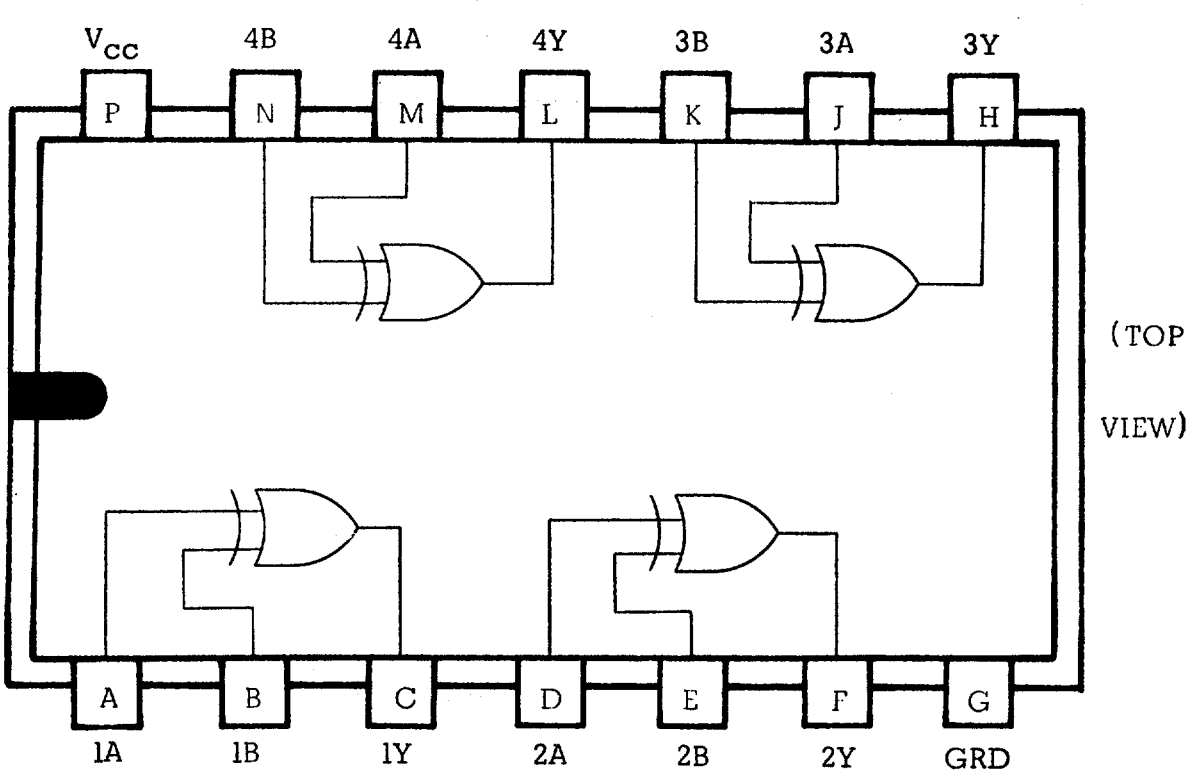
h. Low level to RESET input forces the Q OUTPUT to the high level.

i. Minimum low level pulse width for SET and RESET inputs is 30 nanoseconds.



Dual D Flip-Flop Logic Symbol, Truth Table, and Propagation Delay

8-1.6.11 Integrated Circuit SN7486N Quadruple 2-Input Exclusive OR Gate.



TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7486N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated circuits delineated in paragraph 8-1.3.

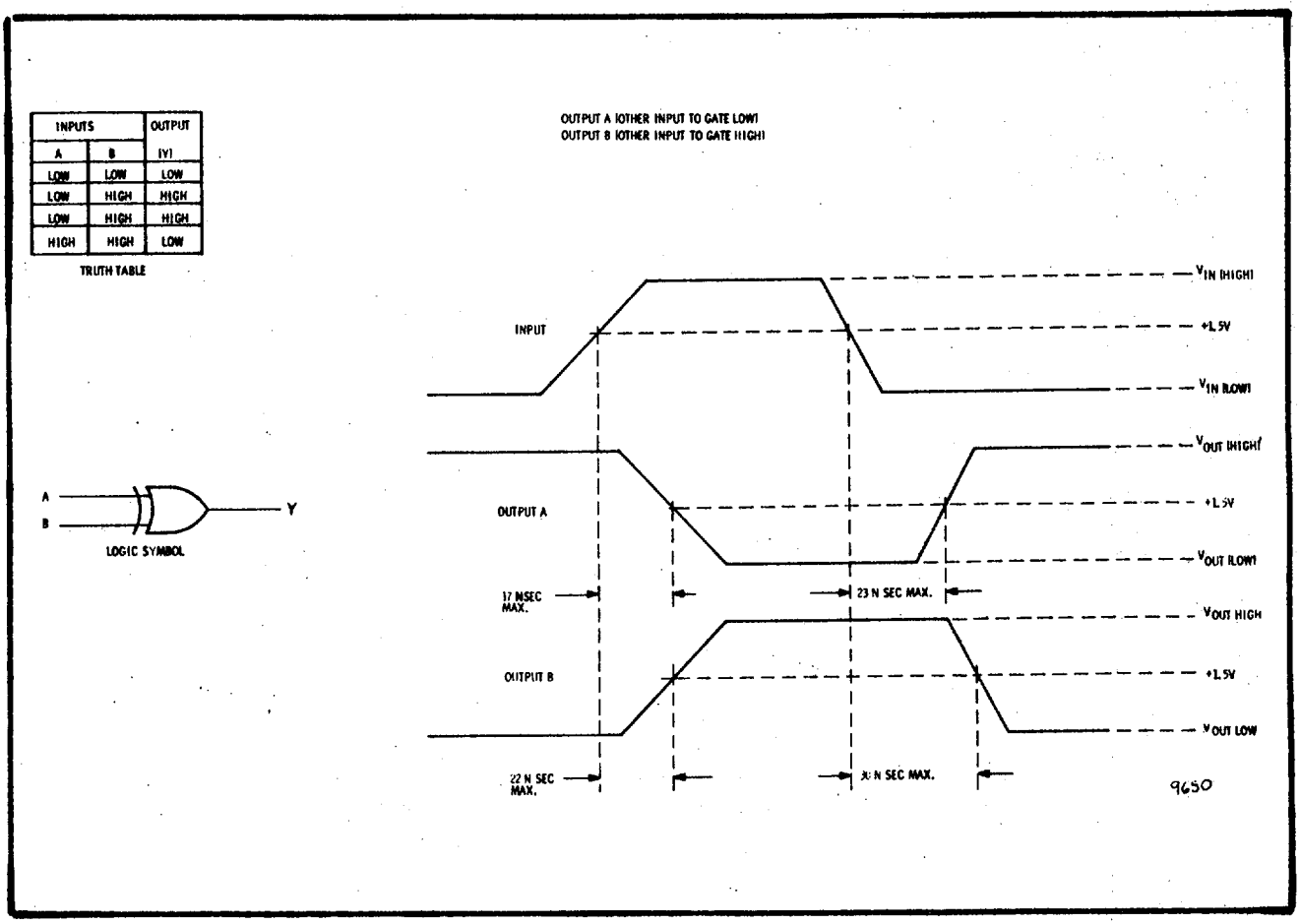
a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive with respect to ground.

c. Output Current: Maximum capability is to accept 16 milliamperes (current sink) when the output is at a low level and to supply 9.1 milliamperes (current source) when the output is at a high level.

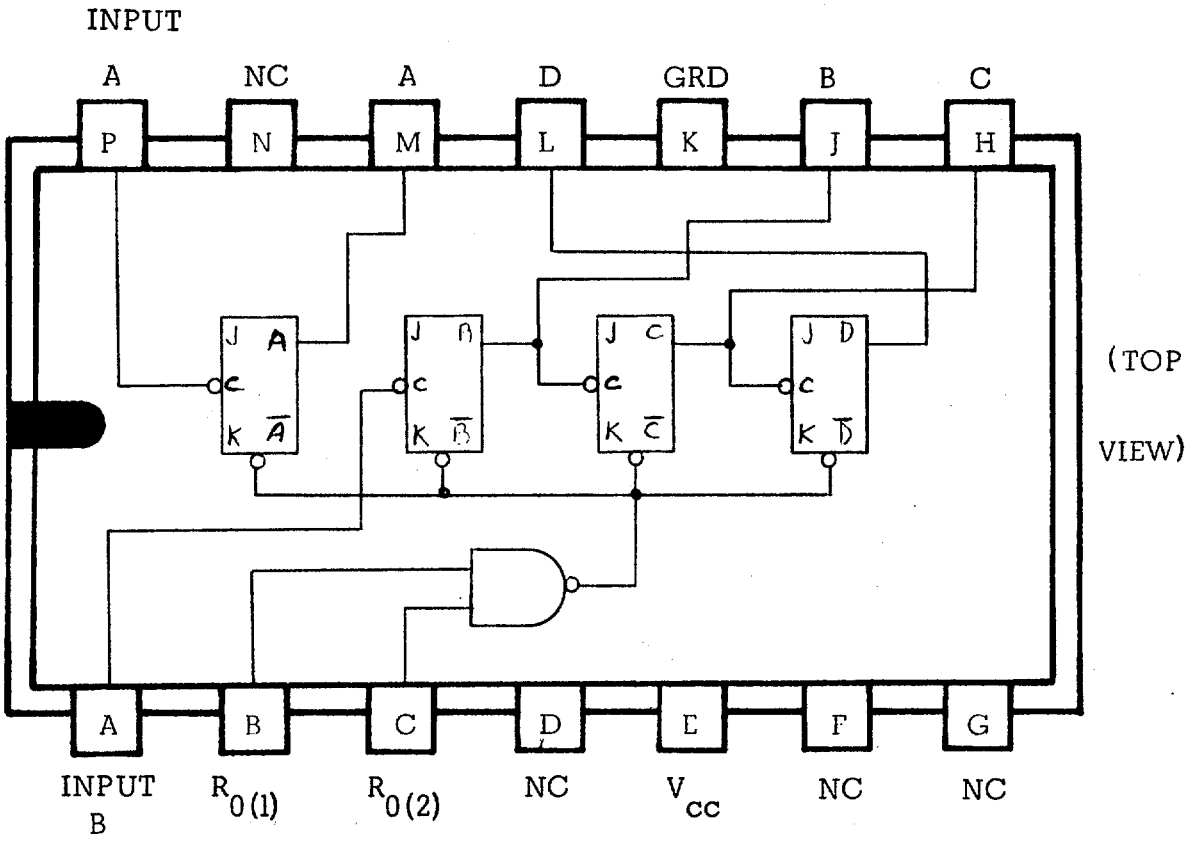
d. No more than one gate output in each pack should be shorted to ground at the same time.

e. Supply Voltage (V_{cc}): Should be +5.0 volts ±5%.



Quadruple 2-Input Exclusive-OR-Gate Logic Symbol, Truth Table, and Propagation Delay

8-1.6.12 Integrated Circuit SN7493N 4-Bit Binary Counter.



DESCRIPTION. The high speed monolithic 4-bit binary counter consists of four master-slave flip-flops which are interconnected to provide a divide-by-two counter and a divide by eight counter. A gated DC (direct) input is provided which inhibits the clock inputs to each flip-flop and sets the outputs to (COUNT = 00002) zero. As the output from flip-flop "A" is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes.

a. When used as a 4-bit ripple through counter, output "A" must be externally connected to input "B". The input clock pulses are connected to input INPUT A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table.

b. When used as a 3-bit ripple through counter, the input clock is connected directly to INPUT B. Simultaneous divisions of 2,4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop "A" is available if the reset function coincides with the reset for the 3-bit ripple counter.

TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7493N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated circuits delineated in paragraph 8-1.3.

a. Input Signal Voltage: Must not exceed +5.5 volts.

b. Input Signal Polarity: Must be positive with respect to ground.

c. Output current: Maximum capability is to accept (sink) 16 milliamperes when the output is at a low level and to supply (source) 9.1 milliamperes when the output is at a high level.

d. No more than one output should be shorted to ground at a time.

e. Supply Voltage: (V_{CC}) should not exceed +7.0 volts.

f. Maximum Clock Frequency: 18 MHz

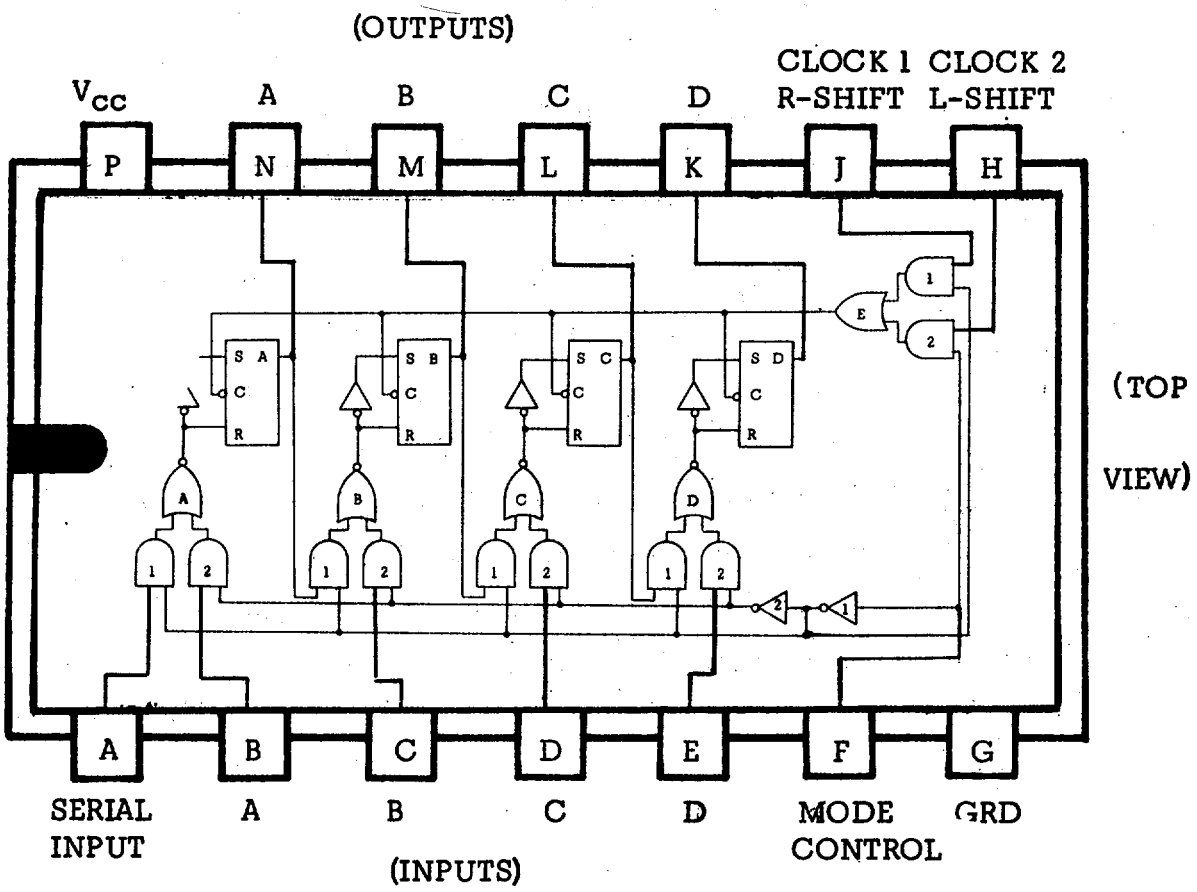
g. Propagation delay time to a logical high level, from input clock pulse is a maximum of 135 nanoseconds.

h. Propagation delay time to a low level from input clock pulse is a maximum of 13,5 nanoseconds.

COUNT	POSITIVE LOGIC OUTPUTS			
	D	C	B	A
0	LOW	LOW	LOW	LOW
1	LOW	LOW	LOW	HIGH
2	LOW	LOW	HIGH	LOW
3	LOW	LOW	HIGH	HIGH
4	LOW	HIGH	LOW	LOW
5	LOW	HIGH	LOW	HIGH
6	LOW	HIGH	HIGH	LOW
7	LOW	HIGH	HIGH	HIGH
8	HIGH	LOW	LOW	LOW
9	HIGH	LOW	LOW	HIGH
10	HIGH	LOW	HIGH	LOW
11	HIGH	LOW	HIGH	HIGH
12	HIGH	HIGH	LOW	LOW
13	HIGH	HIGH	LOW	HIGH
14	HIGH	HIGH	HIGH	LOW
15	HIGH	HIGH	HIGH	HIGH

TRUTH TABLE

8-1.6.13 Integrated Circuit SN7495N 4-Bit Left-Shift Right-Shift Register.



Note: Positive Logic
Mode Control = 0 for right- shift
Mode Control = 1 for left- shift or parallel load

TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN7495N integrated circuit are given below. Refer also to the general characteristics applicable to all digital integrated circuit cards provided at the beginning of this section of the manual.

a. Fan-In. All inputs are one standard load except the mode control which is two standard loads.

b. All unused input pins should be tied to V_{CC}.

c. Input Signal Voltage. +5.5 volts maximum and must be positive with respect to ground.

d. Fan-Out. Each output can drive ten standard loads.

e. Output Current. Maximum capability is to accept 16 ma (current sink) in the logic 0 state and to supply 9.1 ma (current source) on the logic 1 state.

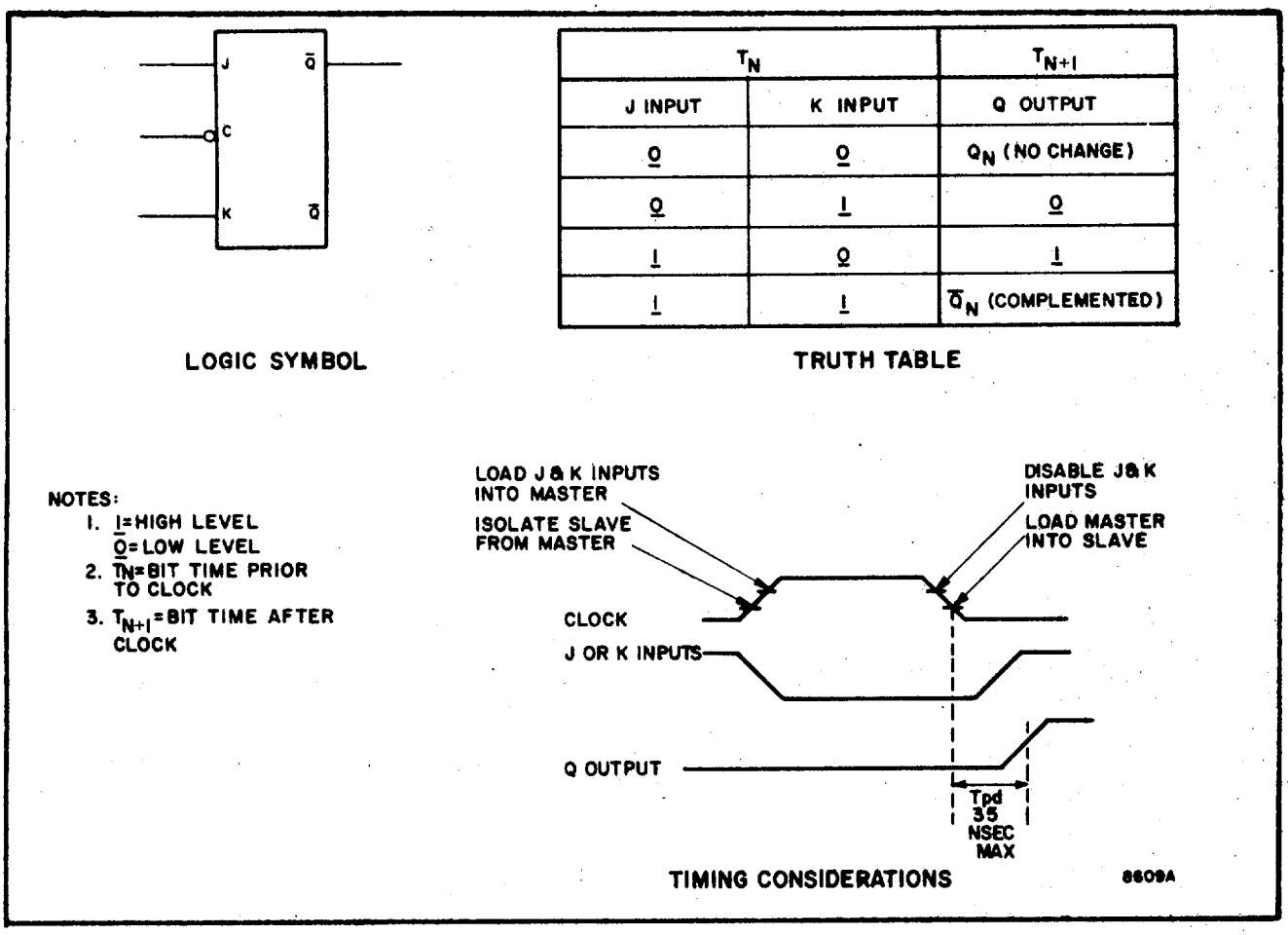
f. No more than one output should be shorted to ground at the same time .

g. Operation of the J-K flip-flops is based on the master-slave principle. Inputs to the flip-flops are controlled by both edges of each clock pulse and this operating sequence is illustrated in the figure below. Other considerations are as follows:

h. Minimum Width of Clock Pulses: 15 nanoseconds.

i. Maximum Shift Frequency: 20 MHz.

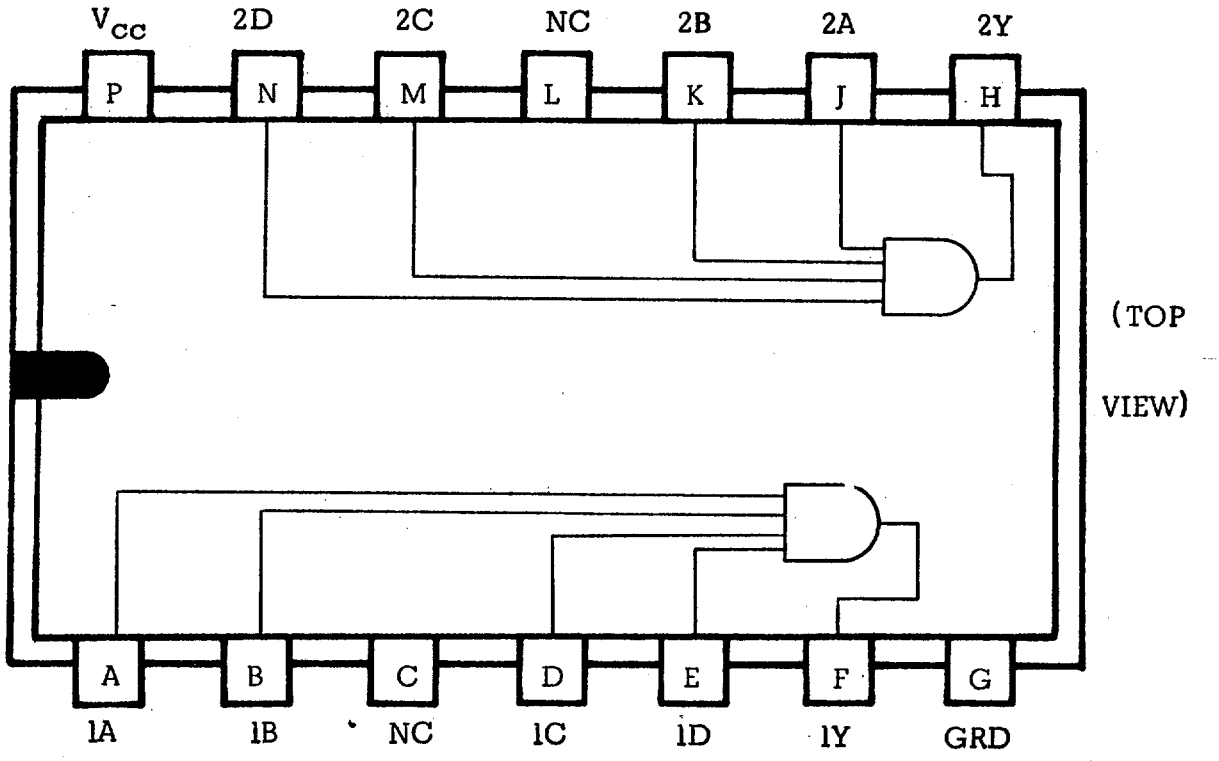
j. Maximum propagation delay time to a logic high or low level from either clock circuit to outputs, T_{pd}, is 35 nanoseconds.



T_N		T_{N+1}
J INPUT	K INPUT	Q OUTPUT
0	0	Q_N (NO CHANGE)
0	1	0
1	0	1
1	1	$\overline{Q}_N$ (COMPLEMENTED)

J-K Master-Slave Logic Symbol, Truth Table, and Timing Considerations

8-1.6.14 Integrated Circuit SN74H21N High Speed Dual 4-Input AND Gate.



TECHNICAL CHARACTERISTICS. The electrical characteristics of the SN74H21N integrated circuit are given below. These characteristics are in addition to the general characteristics pertinent to all digital integrated circuits delineated in paragraph 8-1.3.

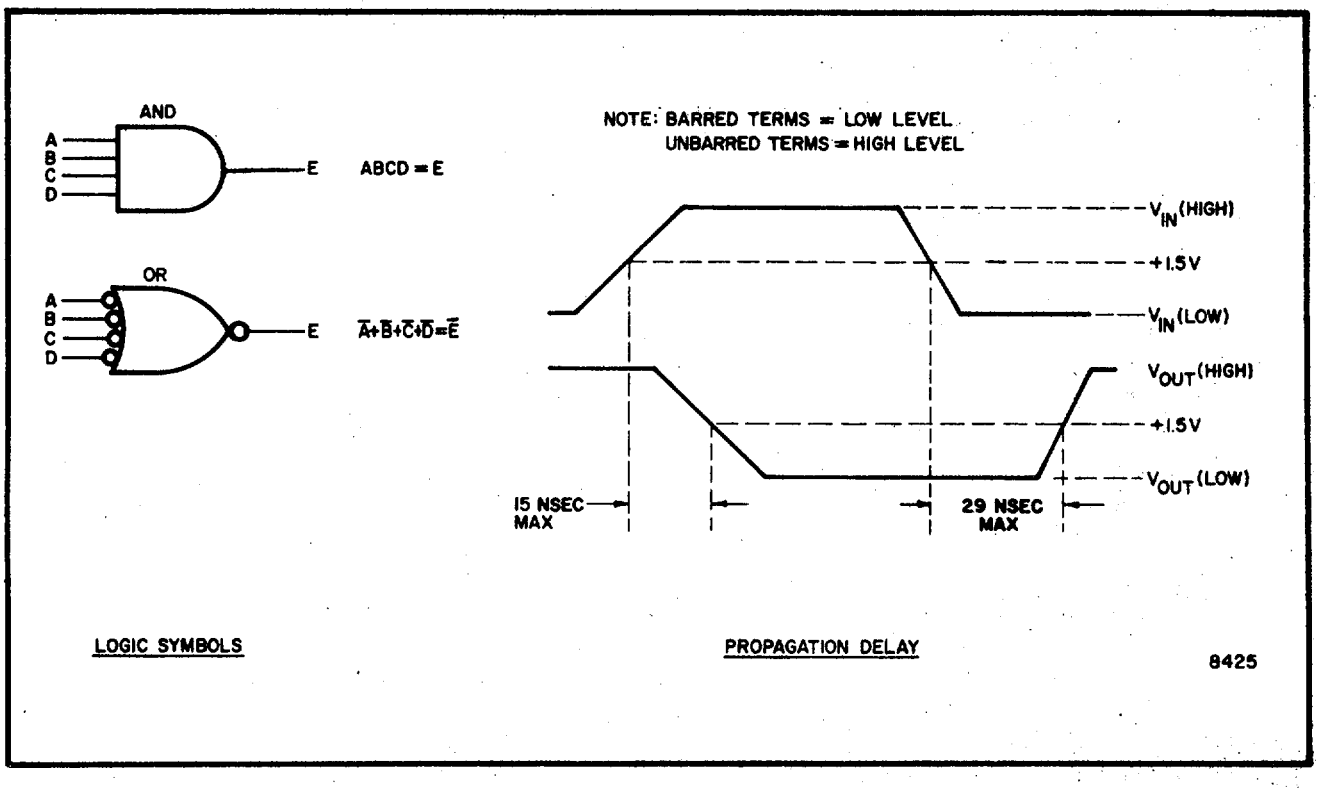
a. Input Signal Voltage: Must not exceed +5.5 volts,

b. Input Signal Polarity: Must be positive with respect to ground.

c. Output Current: Maximum capability is to accept 16 milliamperes (current sink) when the output is at a low level and to supply 9.1 milliamperes (current source) when the output is at a high level.

d. No more than one gate output in each pack should be shorted to ground at the same time.

e. Supply Voltage (V_{CC}): Should be +5.0 volts ±5%.



Four-Input AND Gate Logic Symbols and Propagation Delay

8-1.6.15 Integrated Circuit SN75450 Multi-purpose Interface Circuit.

DESCRIPTION. The two NAND gates are conventional TTL gates -operating from +5 volts and featuring typical propagation delays of 10 nsec. with an average power dissipation of 10 milliwatts per gate. Typical Series 74 input and output characteristics are specified., Each gate has one independent input (IN) and one input common to the other gate (Strobe), See paragraph 8-1.3 for general specifications for TTL integrated circuits.

The two transistors in the SN75450 design feature the capability for sinking up to 250 milliamps with a saturation voltage of less than 400 millivolts. With the emitter of one of the transistors grounded, its base can be driven very effectively directly from the output of one of the NAND gates. This arrangement provides low impedance turn-on and turn-off drive for the transistor. This permits

high speed operation and collector-to-emitter voltages exceeding the collector-to-emitter breakdown of the transistor.

Because the two transistors are fabricated on the same monolithic chip, they exhibit characteristics that are well-matched. It is therefore permissible to parallel the transistor for a 500 milliamp driver application. The NAND gates may also be paralleled for additional drive capability.

8-2. MANUFACTURER 'S CODES.

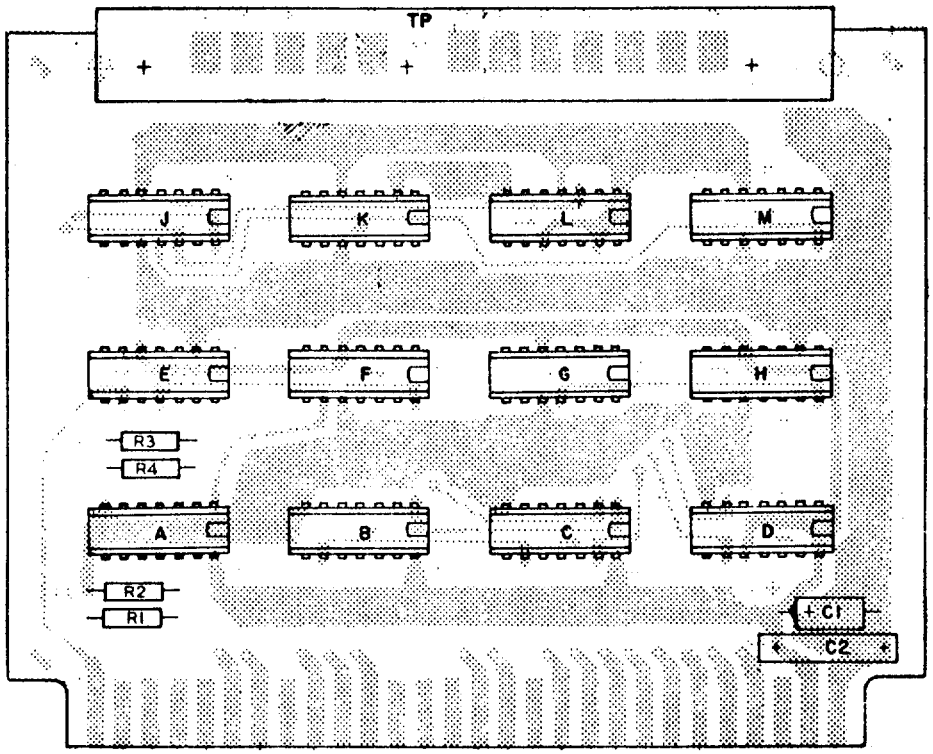
In the parts lists for the printed circuit cards, the manufacturers are identified by federal supply code numbers per cataloging H4-2; a code-to- name index is provided in table 8-1.

Table 8-1. Index to Manufacturer's Codes List

CODE	NAME	ADDRESS
01295	Texas Instruments, Inc. Semiconductor Components Div.	13500 North Central Expressway Dallas, Texas
04713	Motorola Semiconductor Products	505 East McDowell Phoenix, Arizona
05397	Union Carbide-Kemet Dept.	Cleveland, Ohio
06809	Dynatronics, An Operation of the Electro Dynamics Division of General Dynamics	P.O. Box 2566 Orlando, Florida
07263	Fairchild Semiconductor	313 Bayshore Frontage Road Mountain View, California
14655	Cornell-Dubilier Electronic Corp. (CDE)	50 Paris Street Newark, New Jersey
17554	Components, Inc.	Smith Street Biddeford, Maine
19080	Robison Electronics, Inc.	3636 W. 139th St. Hawthorne, California
25088	Seimans of America	350 Fifth Avenue New York, New York
35009	IRC Resistors	Ontario, Canada
	M-Tron Industries	Yankton, S.D. 57078

710-1,-2 CLOCK GENERATOR PRINTED CIRCUIT CARD.

DESCRIPTION. The type 710 printed circuit card contains circuits which comprise the clock generator, test rate selection gates, Self-Test flipflops and lamp driver circuits required for the Card Tester. Operation of the individual logic circuits is fully described in section IV of this manual. Technical characteristics for individual integrated circuit packs contained on this printed circuit board are provided in paragraph 8-1.6. General characteristics for TTL integrated circuits are delineated in paragraph 8-1.3. Printed circuit board component locations are illustrated below and the parts identification and logic diagrams are located on succeeding pages. See Section IX for individual card test information.



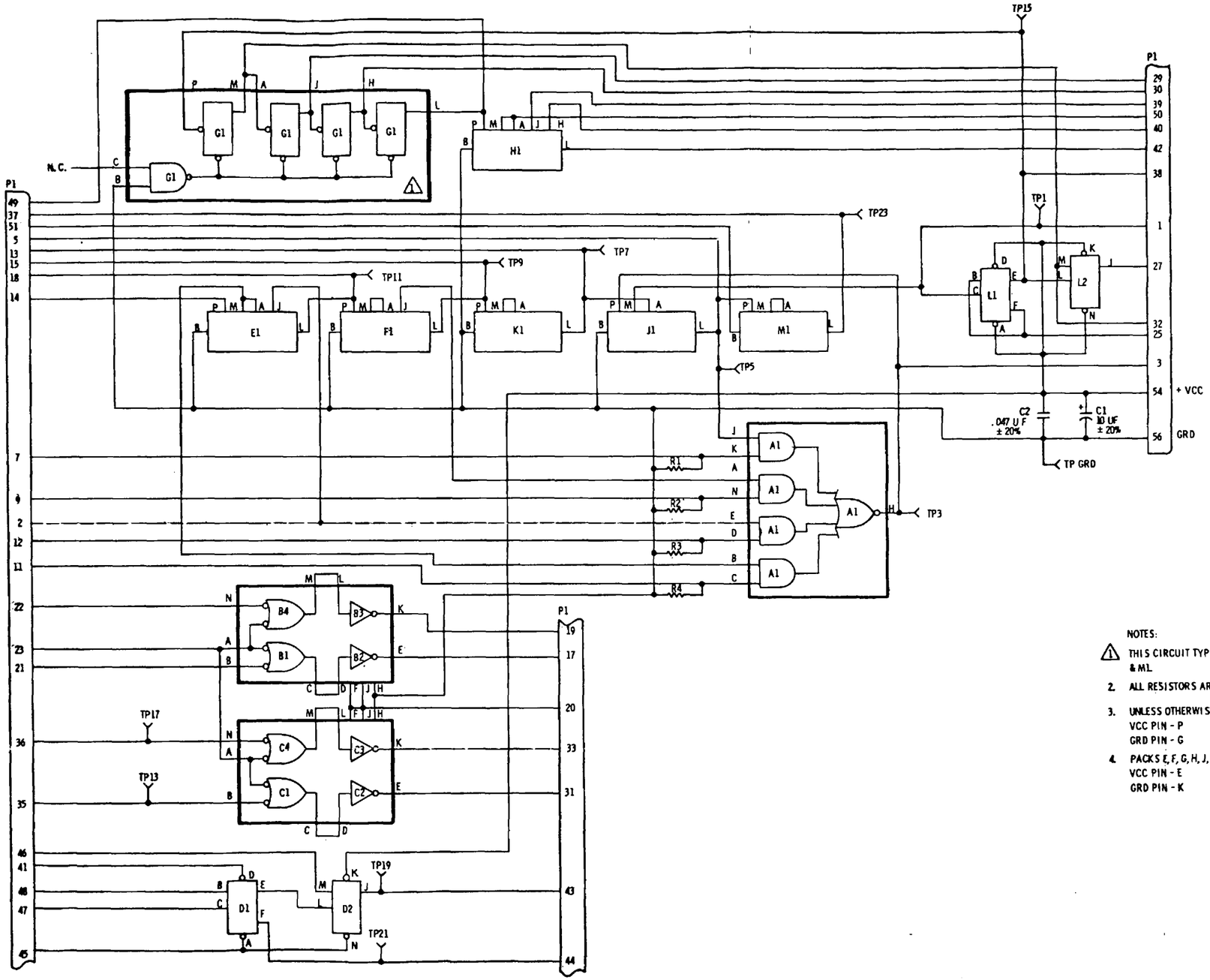
COMPONENT SIDE OF BOARD

08-890710-1 Sh.2-O/R
08-890 710-2 (Not Keyed)

Clock Generator Component Locations

Clock Generator Parts List
(Assembly Drawing 08-890710-1,-2 Sh. 2-O/R)

REF DES	DESCRIPTION	MFG/ CODE/	PART NO.	QTY
C1	CAPACITOR, 10 UF, ±20%, 20V	17554	CL106	1
C2	CAPACITOR, .047 UF, +20%, 400V	25088	B32232-A	1
A	INTEGRATED CIRCUIT PACK 4-WIDE 2-INPUT AND-OR-INVERT GATE	01295	SN7454N	1
B,C	INTEGRATED CIRCUIT PACK DUAL INTERFACE/DRIVER	01295	SN75450N	2
D, L	INTEGRATED CIRCUIT PACK-DUAL D TYPE EDGE TRIGGERED EE	01295	SN7474N	2
E-H,J,K, M	INTEGRATED CIRCUIT PACK-FOUR BIT COUNTER	01295	SN7493N	7
R1-R4	RESISTOR 470 OHM +5% 1/4W	35009	RC07GF471J	4
TP	TEST POINT CONNECTOR	06809	04-000189	1

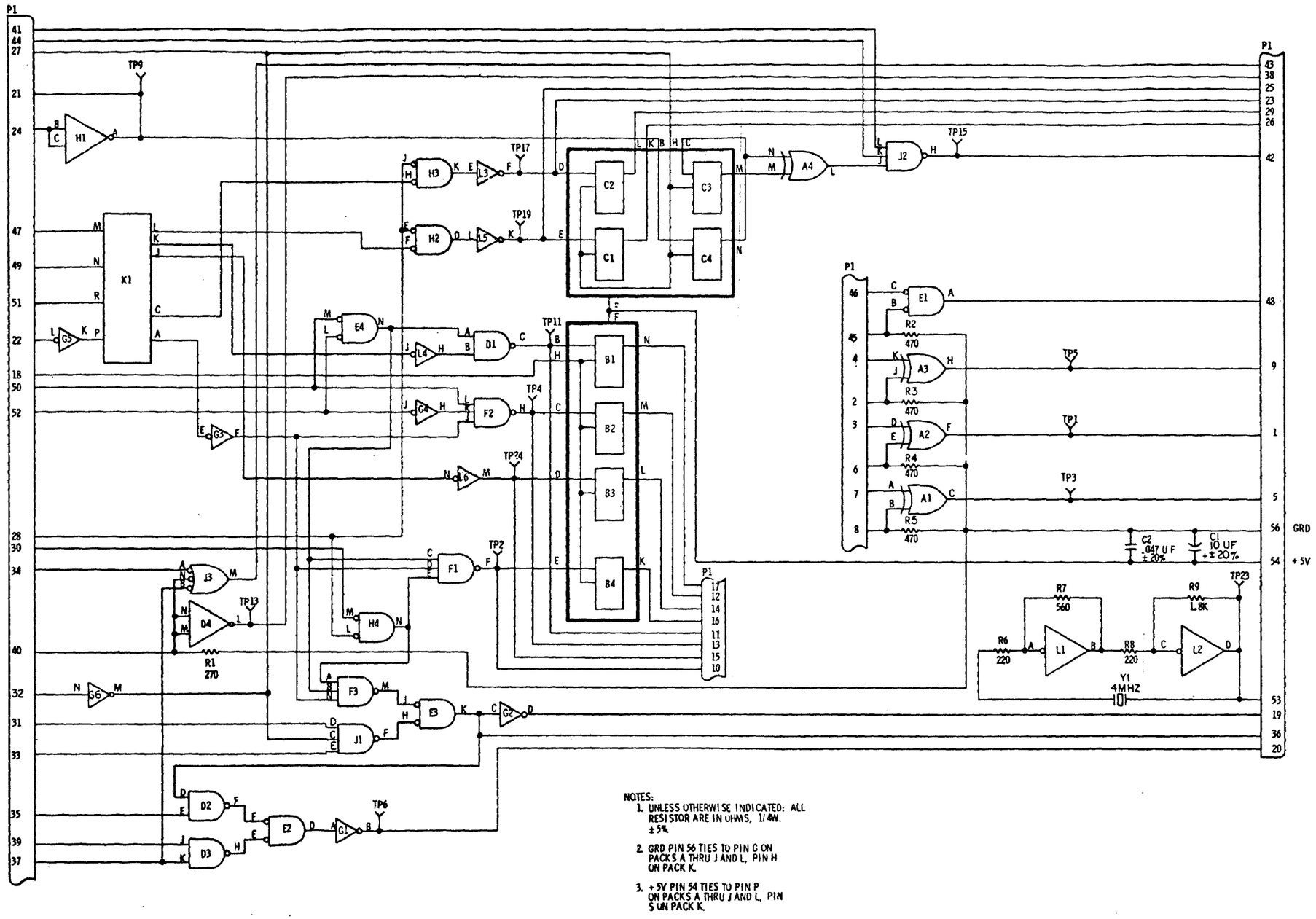


NOTES:

1. THIS CIRCUIT TYPICAL FOR PACKS E1, F1, G1, H1, J1, K1 & M1.
2. ALL RESISTORS ARE 470 OHMS, 1/4W, ± 5%
3. UNLESS OTHERWISE INDICATED PACKS ARE WIRED FOR:
   VCC PIN - P
   GRD PIN - G
4. PACKS E, F, G, H, J, K & M ARE WIRED FOR
   VCC PIN - E
   GRD PIN - K

02-002982-1 O/R

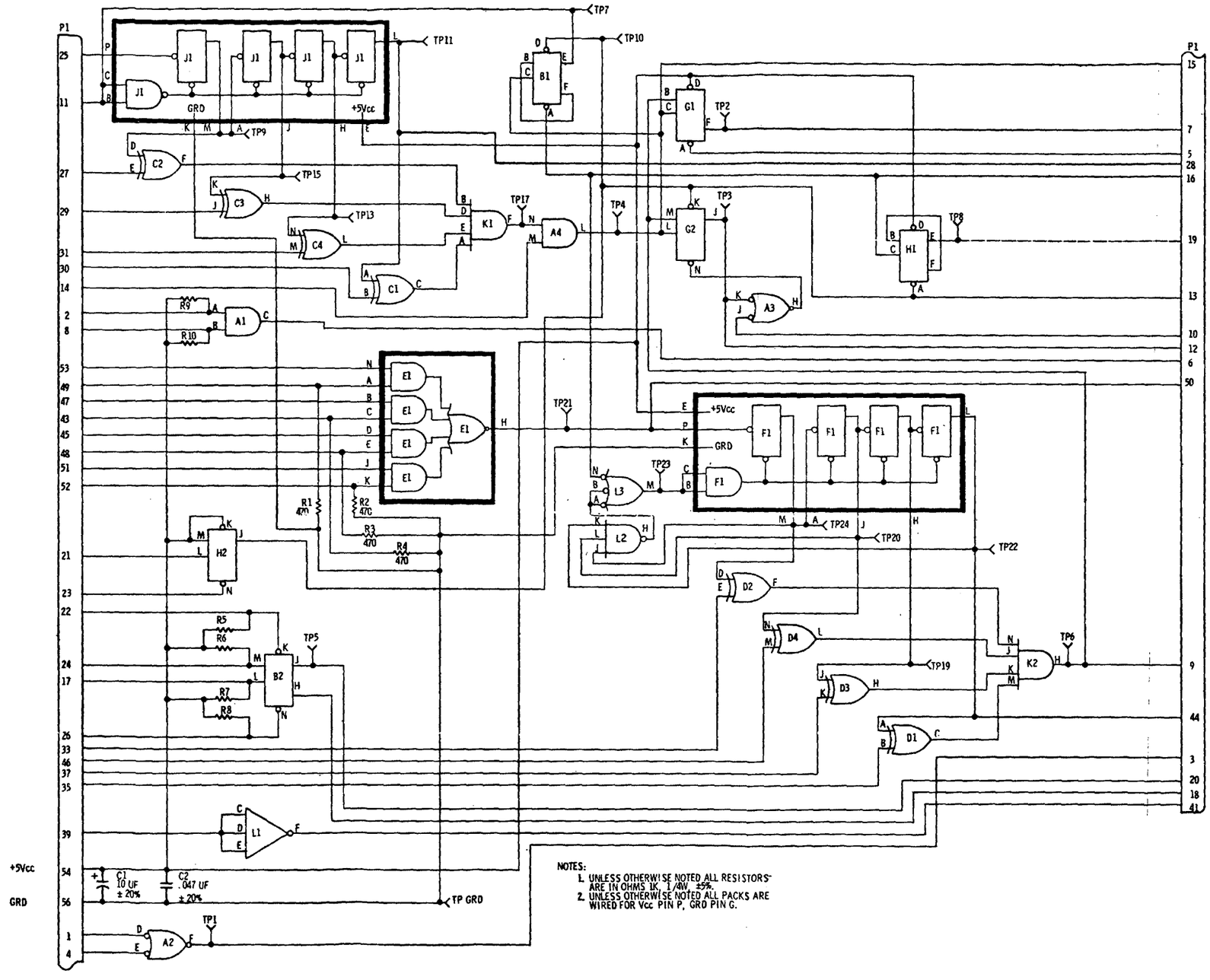
Function Generator Logic Diagram



NOTES:
1. UNLESS OTHERWISE INDICATED: ALL RESISTOR ARE IN OHMS, 1/4W. ±5%
2. GRD PIN 56 TIES TO PIN G ON PACKS A THRU J AND L, PIN H ON PACK K.
3. +5V PIN 54 TIES TO PIN P ON PACKS A THRU J AND L, PIN S ON PACK K.

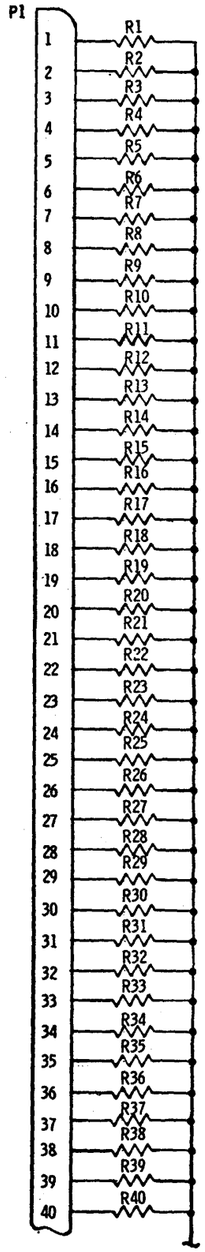
02-002983-1 O/R

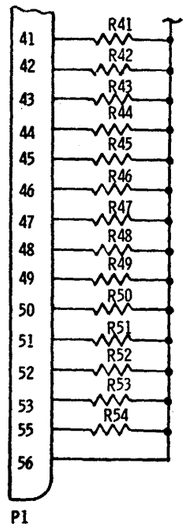
Clock Generator Logic Diagram



02-002984-1 O/R

Go-No-Go Logic Diagram

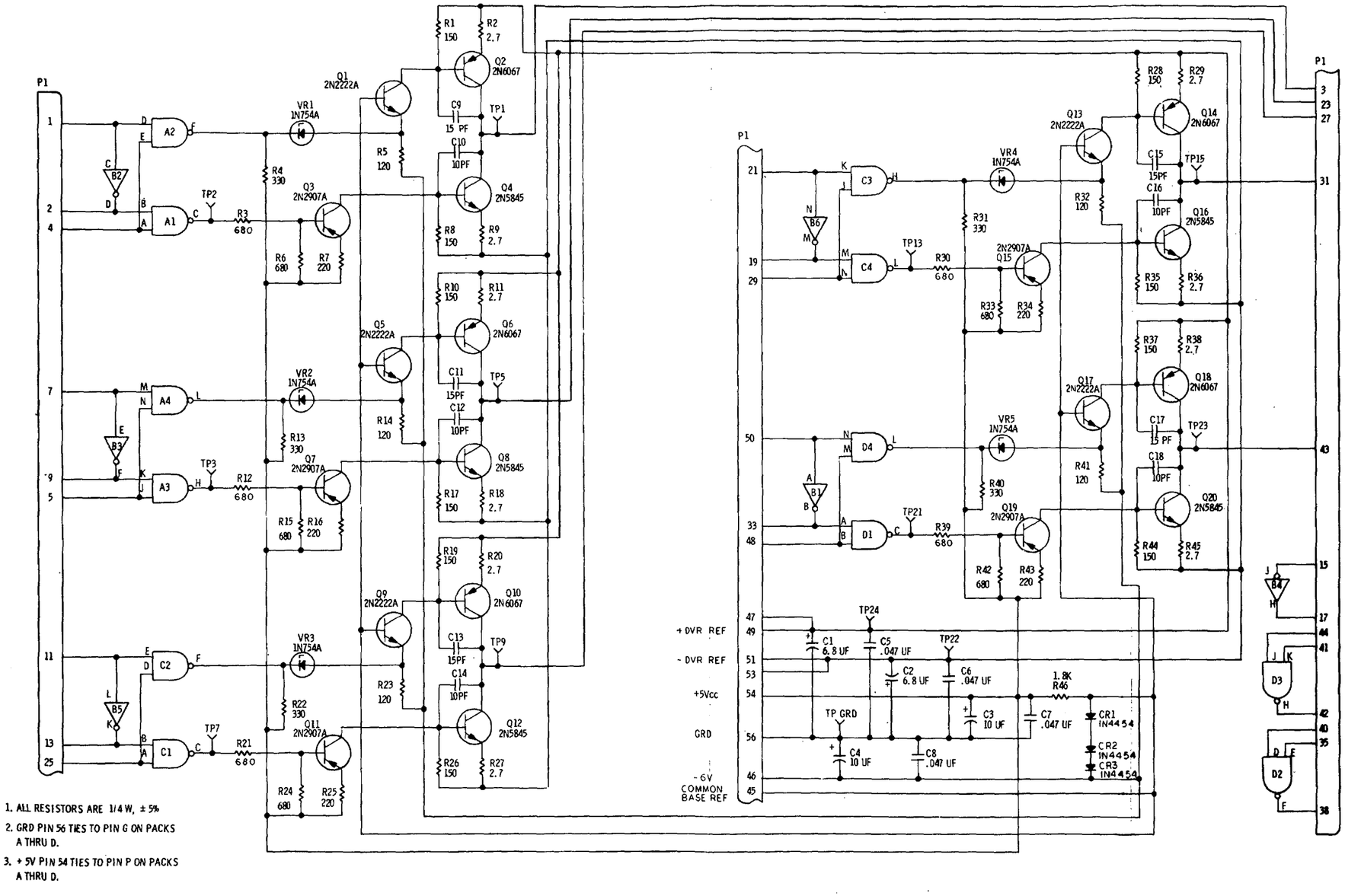




DASH NO.	RESISTOR VALUE
-1	3K Ω, 1/2 W, ± 5%
-2	510 Ω, 1/2 W, ± 5%

02-002979-1 O/R

Resistive Loads Schematic Diagram

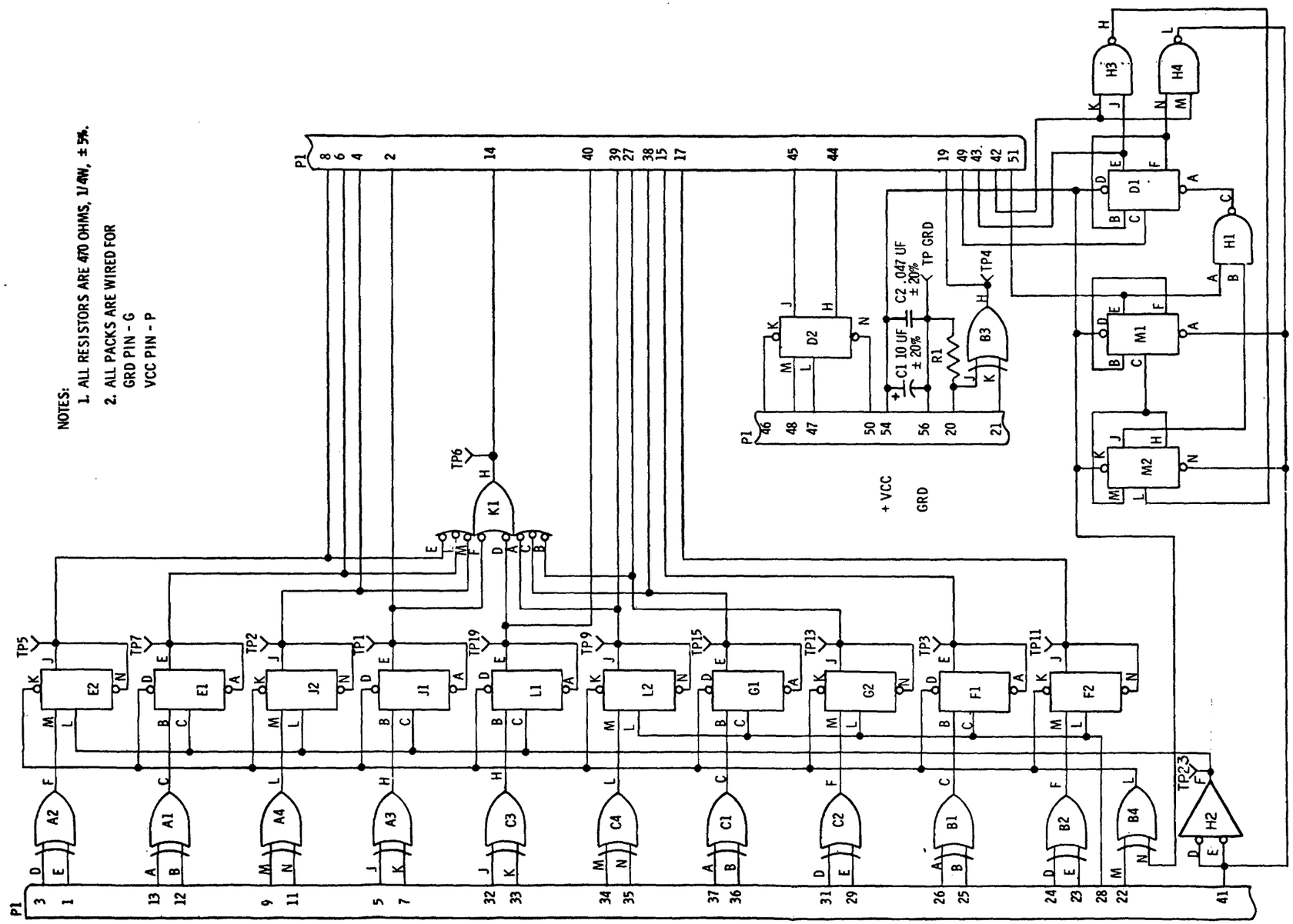


1. ALL RESISTORS ARE 1/4 W, ± 5%
2. GRD PIN 56 TIES TO PIN G ON PACKS A THRU D.
3. + 5V PIN 54 TIES TO PIN P ON PACKS A THRU D.

02-002986-1 B Rev.

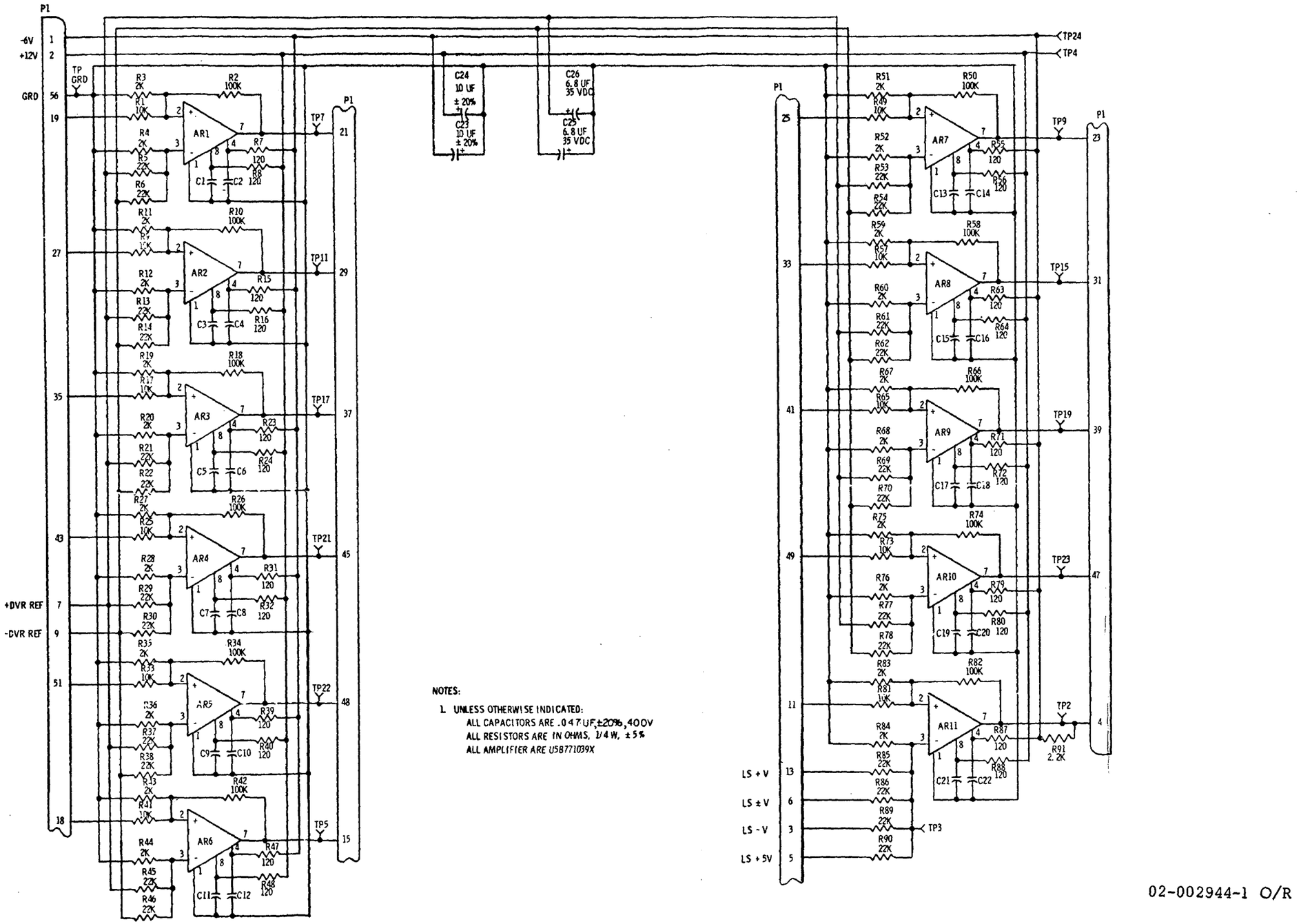
Programmable Driver Schematic Diagram

NOTES:
1. ALL RESISTORS ARE 470 OHMS, 1/4W, ± 5%.
2. ALL PACKS ARE WIRED FOR
   GRD PIN - G
   VCC PIN - P



02-002981-1 O/R

Input Fault Comparater Logic Diagram



NOTES:

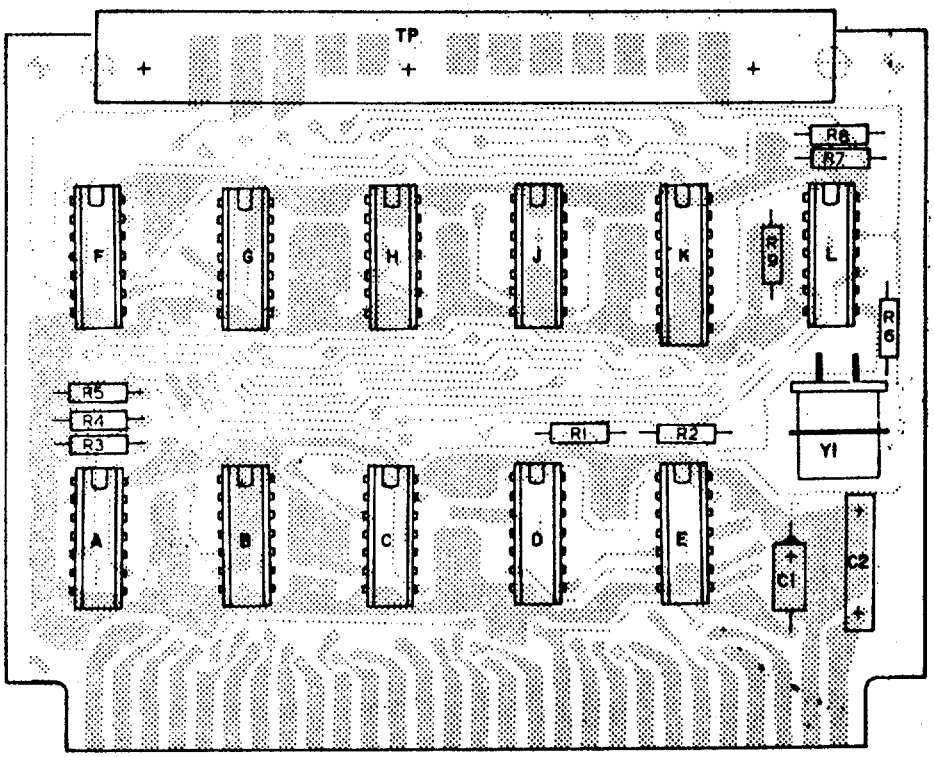
1. UNLESS OTHERWISE INDICATED:
   ALL CAPACITORS ARE .047 UF, ±20%, 400V
   ALL RESISTORS ARE IN OHMS, 1/4W, ±5%
   ALL AMPLIFIER ARE U58771039X

02-002944-1 O/R

Input Level Shifter Schematic Diagram

711-1,-2 FUNCTION GENERATOR PRINTED CIRCUIT CARD.

DESCRIPTION. The type 711 printed circuit board contains several Card Tester circuits consisting of the "C" clock generator, 4MHz oscillator, frame start decoder, edge detector and miscellaneous other digital logic circuits. Individual theory of operation descriptions are provided in section IV of this manual and general technical characteristics are located in paragraph 8-1.3. Detailed technical characteristics pertaining to the individual integrated circuits used in this printed circuit card are given in paragraph 8-1.6. Parts information and component locations are provided below in addition to the logic diagram and test information which is located on succeeding pages.



COMPONENT SIDE OF BOARD

08-890711-1 Sh.2-O/R
08-890711-2 (Not Keyed)

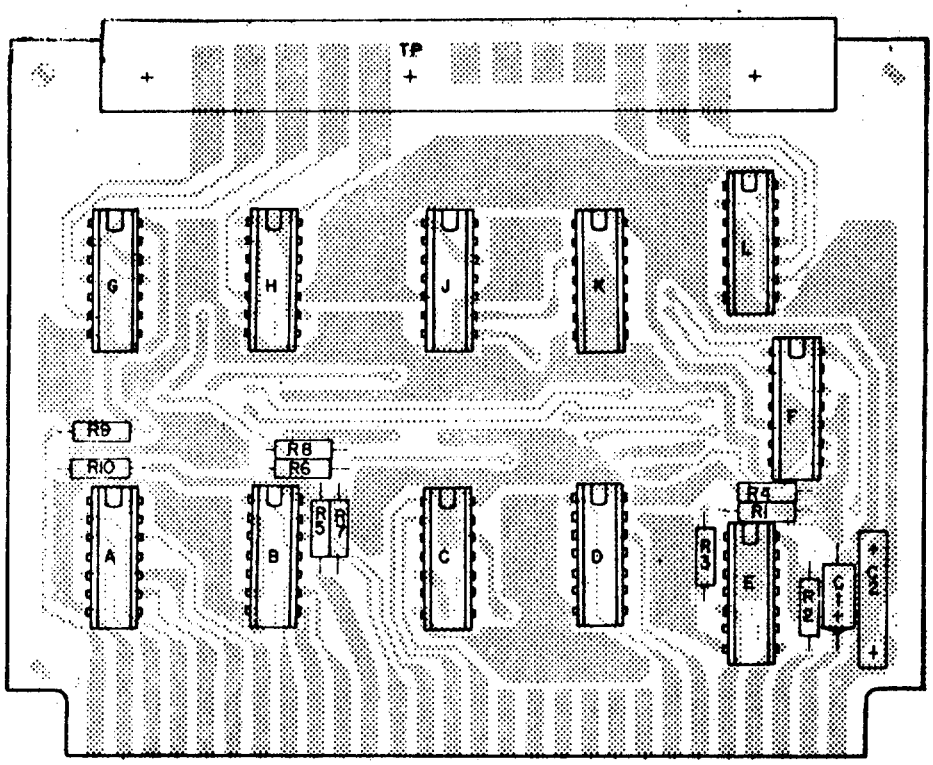
Function Generator Component Locations

Function Generator Parts List
(Assembly Drawing 08-890711-1,-2 Sh. 2-O/R)

REF DES	DESCRIPTION	MPG CODE	PART NO.	QTY
C1	CAPACITOR, 10 UF,+ 20%, 20V	17554	CL106	1
C2	CAPACITOR, 047 UF, + 20%, 400V	25088	B32232-A	1
A	INTEGRATED CIRCUIT PACK-QUAD 2 INPUT EXCLUSIVE OR ELEMENT	01295	SN7486N	1
B,C	INTEGRATED CIRCUIT PACK-4 BIT SHIFT REGISTER	01295	SN7495N	2
D	INTEGRATED CIRCUIT PACK-QUAD 2-INPUT POS NAND GATE	01295	SN7400N	1
E,H	INTEGRATED CIRCUIT PACK-QUAD 2-INPUT POS NOR GATE	01295	SN7402N	2
F,J	INTEGRATED CIRCUIT PACK-TRIPLE 3 INPUT POS NAND GATE	01295	SN7410N	2
G,L	INTEGRATED CIRCUIT PACK-HEX INVERTER	01295	SN7404N	2
K	INTEGRATED CIRCUIT PACK-4 LINE TO 10 LINE DECODER	01295	SN7444N	1
R1	RESISTOR, 160 OHMS, 1/4W, +5%	35009	RC07GF161J	1
R2-R5	RESISTOR, 470 OHMS, 1/4W, +5%	35009	RC07GF471I	4
R6,R8	RESISTOR,' 220 OHMS, 1/4W, +5%	35009	RC07GF221J	2
R7	RESISTOR, 560 OHMS, 1/4W, +5%	35009	RC07GF561I	1
	RESISTOR, 1.8K, 1/4W, +5%	35009	RC07GF182J	1
TP	TEST POINT CONNECTOR	06809	04-000189	1
Y1	CRYSTAL, 4 MHZ,	06809	19-000008-1	1

712-1,-2 GO/NO-GO LOGIC PRINTED CIRCUIT CARD.

DESCRIPTION. The type 712 printed circuit card contains several Card Tester functional circuits consisting of the edge counter, bit counter, GO/ NO-GO flip-flops programmable AND gate, programmable flip-flop, and miscellaneous other logic elements. Operating characteristics for these circuits are described in detail in section IV. General technical characteristics for integrated circuit cards are listed in paragraph 8-1.3 and detailed characteristics for the individual IC packs are provided in paragraph 8-1.6. Component locations and parts information is provided below in addition to the logic diagram which is located on succeeding pages.



COMPONENT SIDE OF BOARD

08-890712-1 Sh.2-O/R
08-890712-2(Not Keyed)

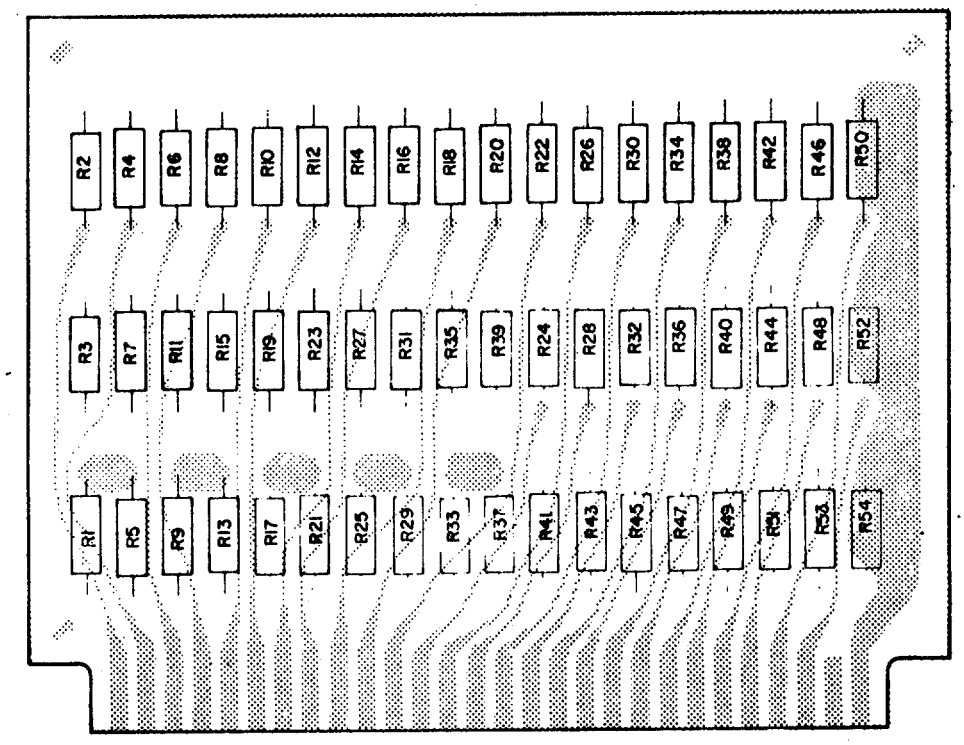
GO/NO-GO Logic Component Locations

GO/NO-GO Logic Parts List
(Assembly Drawing 08-890712-1,-2 Sh. 2-O/R)

REF DES	DESCRIPTION	MFG/ CODE	PART NO.	QTY
C1	CAPACITOR 10 UF ± 20%, 20V	17554	CL106	1
C2	CAPACITOR .047 UF ± 20%, 400V	25088	B32232-A	1
A	INTEGRATED CIRCUIT PACK - QUAD 2-INPUT AND GATE	01295	SN7408N	1
B,G,H	INTEGRATED CIRCUIT PACK - DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP	01295	SN7474N	3
C,D	INTEGRATED CIRCUIT PACK - QUADRUPLE 2 INPUT EXCLUSIVE OR ELEMENT	01295	SN7486N	2
E	INTEGRATED CIRCUIT PACK - 4-WIDE 2 INPUT AND OR INVERT GATE	01295	SN7454N	1
F,J	INTEGRATED CIRCUIT PACK - 4-BIT BINARY COUNTER	01295	SN7493N	2
K	INTEGRATED CIRCUIT PACK - DUAL 4-INPUT AND GATES	01295	SN74H21N	1
L	INTEGRATED CIRCUIT PACK - TRIPLE 3-INPUT NAND GATE	01295	SN7410N	1
R1-R4	RESISTOR, 470 OHMS, 1/4W, ±5%	35009	RC07GF471J	4
R5-R10	RESISTOR, 1K, 1/4W, ±5%	35009	RC07GF102J	6
TP	TEST POINT CONNECTOR	06809	04-000189	1

713-1,-2,-3,-4 PROGRAMMABLE LOAD RESISTOR PRINTED CIRCUIT CARD.

DESCRIPTION. The type 713 printed circuit board contains 54-1/2 watt resistors which provide characteristic loads for the card-under-test output circuits. These load resistors are connected to the output pins via the card reader, ROWS 11 and 12. The dash 1 assembly contains 54-3K ohm resistors and the dash 2 assembly contains 510 ohm resistors. Resistor identification, location, part number, and the logic diagram are provided below.



COMPONENT SIDE OF BOARD

08-890713-1-2 Sh.2-O/R
08-890713-3-4(Not Keyed)

Programmable Load Resistor Component Locations

Programmable Load Resistor Parts List
(Assembly Drawing 08-8;90713-1,-2,-3,-4 Sh.2-O/R)

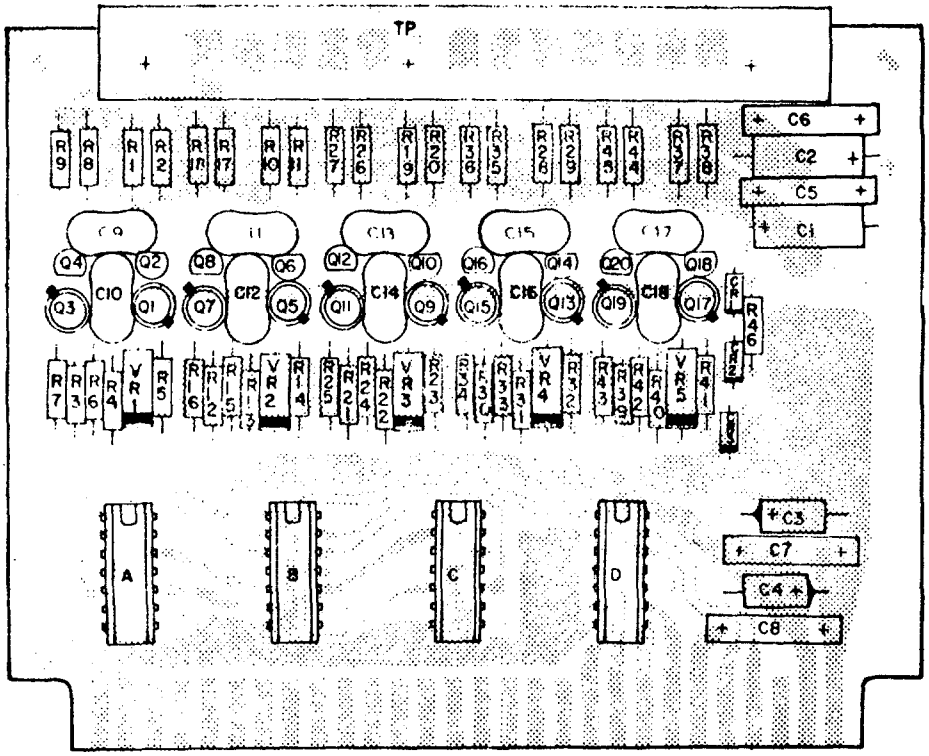
REF DES	DESCRIPTION	MFG/ CODE	PART NO.	QTY
R1-R54 (-1,-3 assembly)	RESISTOR 3K, 1/2W, +5%	35009	RC20GF302J	54
R1-R54 -2,-4 assembly)	RESISTOR 510 OHMS, 1/2W, +5%	35009	RC20GF511J	54

714-1,-2 PROGRAMMABLE DRIVER PRINTED CIRCUIT CARD.

DESCRIPTION. The type 714 printed circuit card contains ten programmable line drivers, two 2-input NAND gates and one inverter logic element. Each of the ten programmable drivers have gating element inputs for controlling the input signal into the drivers. These elements are basic digital logic elements with the technical characteristics delineated in paragraphs 8-1.3 and 8-1.6 for the type SN7400N and SN7404N integrated circuits. Component locations and parts information is provided below in addition to the logic/schematic diagram which is located on succeeding pages.

THEORY OF OPERATION. Each of the ten programmable line drivers have identical operational characteristics and the following description of this operation is with reference to programmable driver number 1, located in the upper left hand corner of the schematic diagram shown on a succeeding page. Driver number 1 consists of gates A1, A2, and B2 and transistors Q1, Q2, Q3, and Q4. Under typical conditions, a high logic signal is applied to pin D of 2-input NAND gate A2 which trues the gate, that is, if the inhibit line (input pin 4) is at a high logic level. Trueing gate A2,, a low level output (A2-F), results in turning Q2 and Q4 off and the driver output changes to a value approximately equal to the positive reference voltage connected to pin 49 of the printed circuit card. With a low level into input pin 1, Q2 turns off and Q4 turns on so that the output of the driver switches to a value approximately equal to the voltage input to -DVR REF, pin 51. For this example, assume that +DVR REF is connected to +10.0 volts and -DVR REF is connected to -10.0 volts. These voltages provide a bi-polar output signal between -10.0 and +10.0 volts, less the voltage drop across Q2 and Q4. A high level into input pin 1 trues NAND gate A2, causing zener diode VR1 to see approximately +0.2 volts on the cathode end. This causes VR1 to cut off and the emmiter of transistor Q1 equals approximately -6.0 volts. The base of Q1 is biased at approximately -4.0 volts from the voltage developed at the CR1 and R46 junction, lower right hand corner of the schematic diagram. With -4.0 volts on the base and -6.0 volts on the emitter, Q1 is biased ON, to supply base current to the

base of transistor Q2, This saturates the transistor Q2 and causes the collector to switch to approximately +9.7 volts. The lower leg of the driver Q4 is OFF for this condition. With a low level input to pin 1, Q2 is biased OFF and Q4 is saturated causing the output of the driver to change to -9.7 volts. For example, a low level into pin 1 trues NAND gate AI, -biases Q3 on, and biases Q4 ON to provide the negative voltage on the collector of Q4 for a low level input.



COMPONENT SIDE OF BOARD

08-890714-1 Sh.2-O/R
08-890714-2(Not Keyed)

Programmable Driver Component Locations

Programmable Driver Parts List
(Assembly Drawing 08-890714-1,-2 Sh.2-O/R)

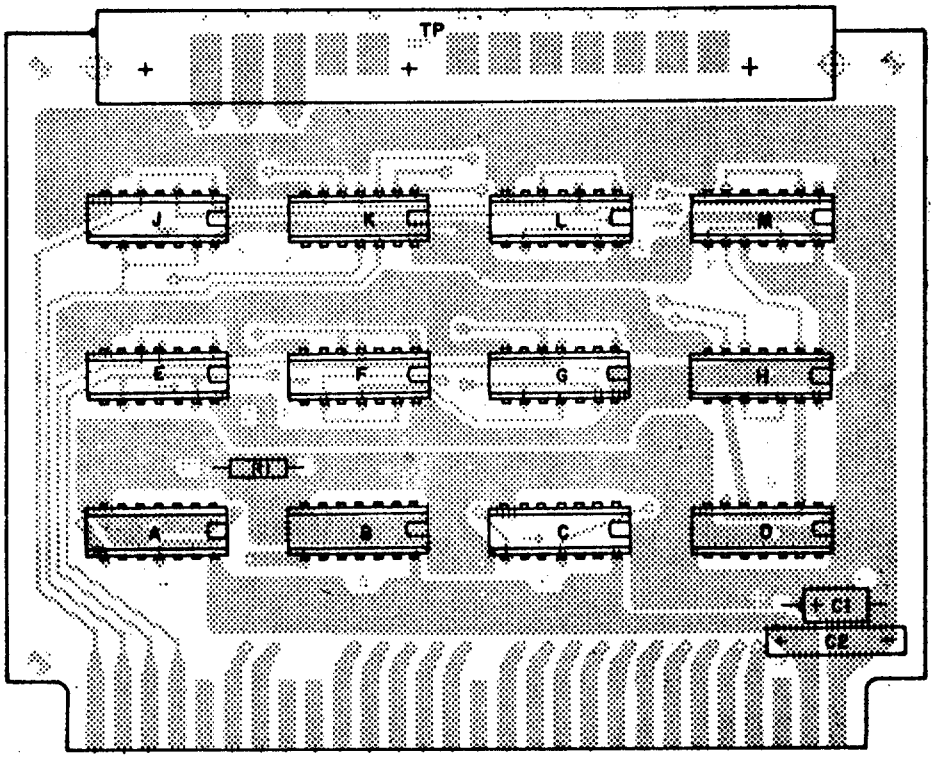
REF DES	DESCRIPTION	MFG/ CODE	PART NO.	QTY
Cl-C2	CAPACITOR, 6,8 UF,35V	05397	T310B6R8K035AS	2
C3-C4	CAPACITOR, 10 UF, ± 20%, 20V	17554	CL106	2
C5-C8	CAPACITOR, .047 ± 20%, 400V	25088	B32232-A	4
C9 C11, 13 C15,17	CAPACITOR, 15 PF ± 5%, 500V	14655	DM15F150J	S
C10, C12,14 C16,18	CAPACITOR, 10 PF ± 5%, 500V	14655	DM15F100J	5
CR1-CR3	DIODE	01295	IN4454	3
A,C,D	INTEGRATED CIRCUIT PACK - QUAD 2-INPUT NAND GATE	01295	SN7400N	3
B	INTEGRATED CIRCUIT PACK - HEX INVERTER	01295	SN7404N	1
Q1 Q5,9 Q13,17	TRANSISTOR, NPN	04713	2N2222A	5
Q2, Q6,10 Q14,18	TRANSISTOR, PNP	04713	2N6067	5.
Q3, Q7,11 Q15,19	TRANSISTOR, PNP	04713	2N2907A	5
Q4 Q8,12 Q16,20	TRANSISTOR, NPN	04713	2N5845	5

Programmable Driver Parts List
(Assembly Drawing 08-890714-1,-2 Sh.2-O/R)

REF DES	DESCRIPTION	MFG/ CODE	PART NO.	QTY
R1,8 R10,17 R19, 26 R28,35 R37,44	RESISTOR, 150 OHMS, 1/4W, +5%	35009	RC07GF151J	10
R2, 9 R11, 18 R20,27 R29,36 R38,45	RESISTOR, 2.7 OHMS, 1/4W, + 5%	35009	RC07GF2R7J	10
R3,6 R12,15 R21, 24 R30,33 R39,42	RESISTOR, 680 OHMS, 1/4W ±5%	35009	RC07GF681J	10
R4 R13,22 R31,40	RESISTOR, 330 OHMS, 1/4W ±5%	35009	RC07GF331J	5
R5 R14,23 R32,41	RESISTOR, 120 OHMS, 1/4W, ±5%	35009	RC07GF121J	5
R7 R16,25 R34,43	RESISTOR, 220 OHMS, 1/4W ±5%	35009	RCOGF221J	5
R46	RESISTOR, 1.8K 1/4W, ±5%	35009	RC07GF182J	1
TP	TEST POINT CONNECTOR	06809	04-000189	1
VR1-VR5	DIODE ZENER	01295	IN754A	5
3	TRANSIPAD (T018 TRANSISTORS)	19080	RC-T018060-2A	10

715-1,-2 INPUT FAULT COMPARATOR PRINTED CIRCUIT CARD.

DESCRIPTION. The type 715 printed circuit board contains the Card Tester input fault comparater logic circuits. These circuits consist of digital logic circuit elements which are fully described in section IV of this manual. Paragraph 8-1.3 provides the general technical characteristics pertinent to TTL integrated circuits and paragraph 8-1.6 provides the individual technical characteristics for each element located on the 715-1 PC card. Component locations, parts information and manufacturers information pertaining to this card are given below. The logic diagram is located on succeeding pages. See Section IX for test information pertinent to this card.



COMPONENT SIDE OF BOARD

08-890715-1 Sh.2-O/R
08-890715-2(Not Keyed)

Input Fault Comparator Component Locations

Input Fault Comparator Parts List
(Assembly Drawing .08- 890715-1, - 2 Sh. 2-O/R)

REF DES	DESCRIPTION	MFG/ CODE	PART NO.	QTY
C1	CAPACITOR, 10 UF, ± 20%, 20V	17554	CL106	1
C2	CAPACITOR, .047 UF ± 20%, 400V	25088	B32232-A	1
A,B,C	INTEGRATED CIRCUIT PACKS-QUAD 2-INPUT EXCLUSIVE-OR	01295	SN7486N	3
D,E,F, G,J,L, M	INTEGRATED CIRCUIT PACKS-DUAL D TYPE EDGE TRIGGERED FLIP-FLOP	01295	SN7474N	7
H	INTEGRATED CIRCUIT PACKS-QUAD 2-INPUT NAND GATE	01295	SN7400N	1
K	INTEGRATED CIRCUIT PACKS-8-INPUT NAND GATE	01295	SN7430N	1
R1	RESISTOR, 470 OHMS, 1/4W,±5%	35009	RC07GF471J	1
TP	TEST POINT CONNECTOR	06809	04-000189	1

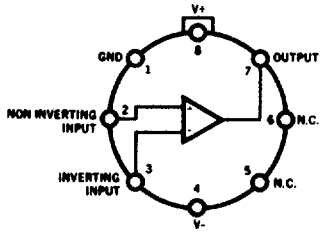
716-1,-2 INPUT LEVEL SHIFTER PRINTED CIRCUIT CARD.

DESCRIPTION. The type 716 printed circuit card contains eleven level shifters which provide a TTL compatible output signal from an input signal which operates over a range from ±1.0 volts through ±26.1 volts. Ten of the level shifters are controlled directly from the programmable power supply source and the remaining level shifter, AR11, is controlled from four individual inputs as described below. Basically the level shifter consists of a high-speed differential comparator which is used to shift the level of the input to standard integrated circuit levels.

TECHNICAL CHARACTERISTICS (uA710) The Fairchild uA710 highspeed differential comparator TO-99 connection diagram and schematic diagram are illustrated below:

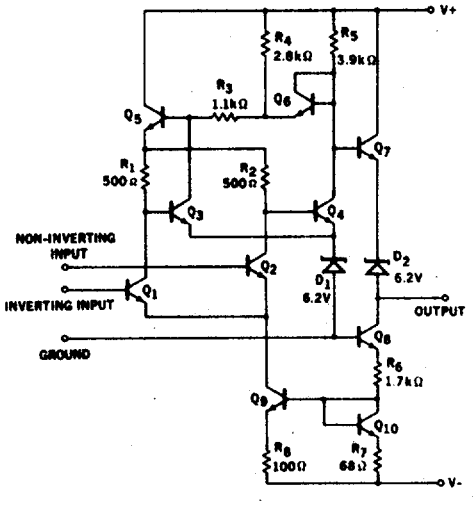
TO-99 CONNECTION DIAGRAM

(TOP VIEW)



Note: Pin 4 connected to case

SCHEMATIC DIAGRAM



Absolute Maximum Ratings:

Positive Supply Voltage - +14.0V

Negative Supply Voltage - -7.0V

Peak Output Current - 10 mA

Differential Input Voltage - ±5.0 V

Input Voltage - ±7.0 V

The uA710 has a voltage gain of 1700.

THEORY OF OPERATION. Each of the eleven level shifters is connected to the +12 volt power supply (comparator pin 8) and the -6 volt power supply (comparator pin 4). The switching threshold is controlled by the voltage levels applied to the +DVR REF and -DVR REF voltage inputs to the printed circuit card, shown in the schematic diagram (D2944) on succeeding pages. The resistor divider network connected to the (-) input to each comparator provides a switching threshold equal to one-half the difference voltage of the + and DVR REF voltages applied to pins 7 and 9 of the card. Comparator AR1 is used as a typical example of level shifter operation and is connect as follows. Pin 19 is the input pin into the comparator and the signal applied to this pin causes the comparator to change states when the input signal voltage reaches one-half the difference between + and DVR REF, For a high level input (voltage of input signal is greater than the threshold voltage) the output signal on pin 21 equals approximately +4.0 volts. A low level input signal provides an output approximately equal to +0.2 volts.

Level shifter AR11's switching threshold is controlled from four individual input pins (3,5,6, and 13). The following formulas are used to determine the threshold point for AR11

$V_t = 1/2\ V_1$

$V_t = 6/13\ (V_1 + V_2)$
$V_t = 6/14\ (V_1 + V_2 + V_3)$

$V_t = 6/15 (V_1 + V_2 + V_3 + V_4)$

WHERE:

V_t = Threshold Voltage

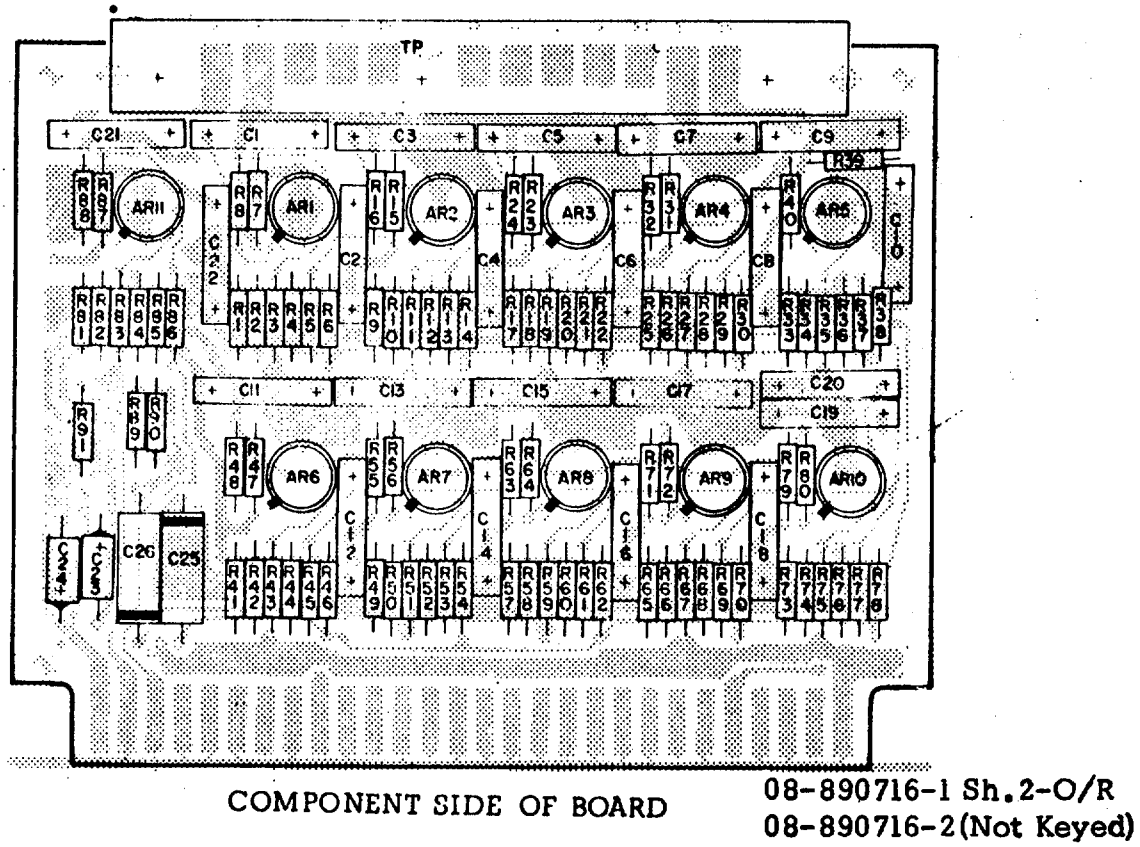
V_1 , Any one power supply voltage connected to any one of the four input pins.

V_2 = Any second power supply voltage connected to any of the remaining three input pins.

V_3 = Any third power supply voltage connected to either of the two remaining input pins.

V_4 = Any fourth power supply voltage connected to the remaining input pin.

With no power supply voltages programmed into the level shifter the threshold voltage equals OV.



Input Level Shifter Component Locations

Input Level Shifter Parts List
(Assembly Drawing 08-890716-1,-2 Sh.2-O/R)

REF DES	DESCRIPTION	MFG/ CODE	PART NO.	QTY
AR1-11	HIGH-SPEED DIFFERENTIAL COMPARATOR	07263	U5B771039X	11
C1-22	CAPACITOR, .047 UF, + 20%,400V	25088	B32232-A	22
C23,24	CAPACITOR, 10 UF, ±20%, 20V	17554	CL106	2
C25,26	CAPACITOR, 6.8 UF, 35VDC	05397	T310B6R8K-035AS	2
R1,9,17 25,33,41 49,57,65 73, 81	RESISTOR, 10,K, 1/4W, ±5%	35009	RC07GF103J	11
R2,10,18 26,34,62 50,58,66 74,82	RESISTOR, 100K, 1/4W, ±5%	35009	RCO7GF104J	11
R3,4,11 12,19,20 27,28,35 36,43,44 51,52,59 60,67,68 75,76,83 84	RESISTOR, 2K, 1/4W, ±5%	35009	RC07GF202J	22
R5,6,13 14,21,22 29,30,37 38,45,46 53,54,61 62,69,70 77,78,85 86,89,90	RESISTOR 22K, 1/4W, ±5%	35009	RC07GF223J	24

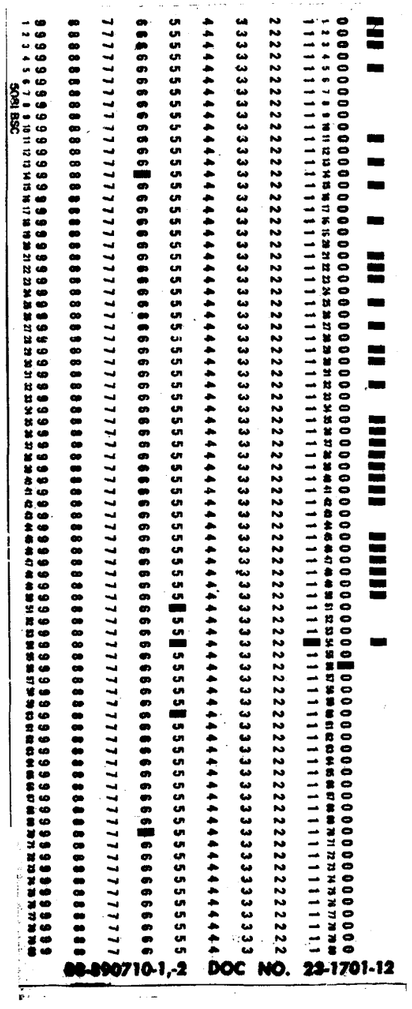
Input Level Shifter Parts List (Cont'd)
(Assembly Drawing 08-890716-1,-2 Sh.2-O/R)

REF DES	DESCRIPTION	MFG/ CODE	PART NO.	QTY
R7, 8,15 16,23,24 31,32,39 40,47,48 55,56, 63 64,71,72 79,80,87 88	RESISTOR, 120 OHMS, 1/4W, ±5%	35009	RC07GF121J	22
R91	RESISTOR, 2.2K, 1/4W ±5%	35009	RC07GF222J	1
TP	TEST POINT CONNECTOR	06809	04-00018-9-	1
3	TRANSIPAD (AR1 - AR11)	19080	RC-TO5030-2A	11

SECTION IX
PRINTED CIRCUIT CARD
TEST PROGRAM

9-1 INTRODUCTION.

Section IX provides the necessary information for testing the internal Card Tester electrical circuits contained on printed circuit cards. This information includes individual schematic diagrams (containing programmed test signals) and test waveforms for each printed circuit card. The test information provided in this section is used in conjunction with program cards, supplied with the manual, and a second Card Tester to isolate malfunctions within the PC cards. Section III, paragraph 3-4, provides the detailed steps necessary to exercise the printed circuit card(s) to be tested.

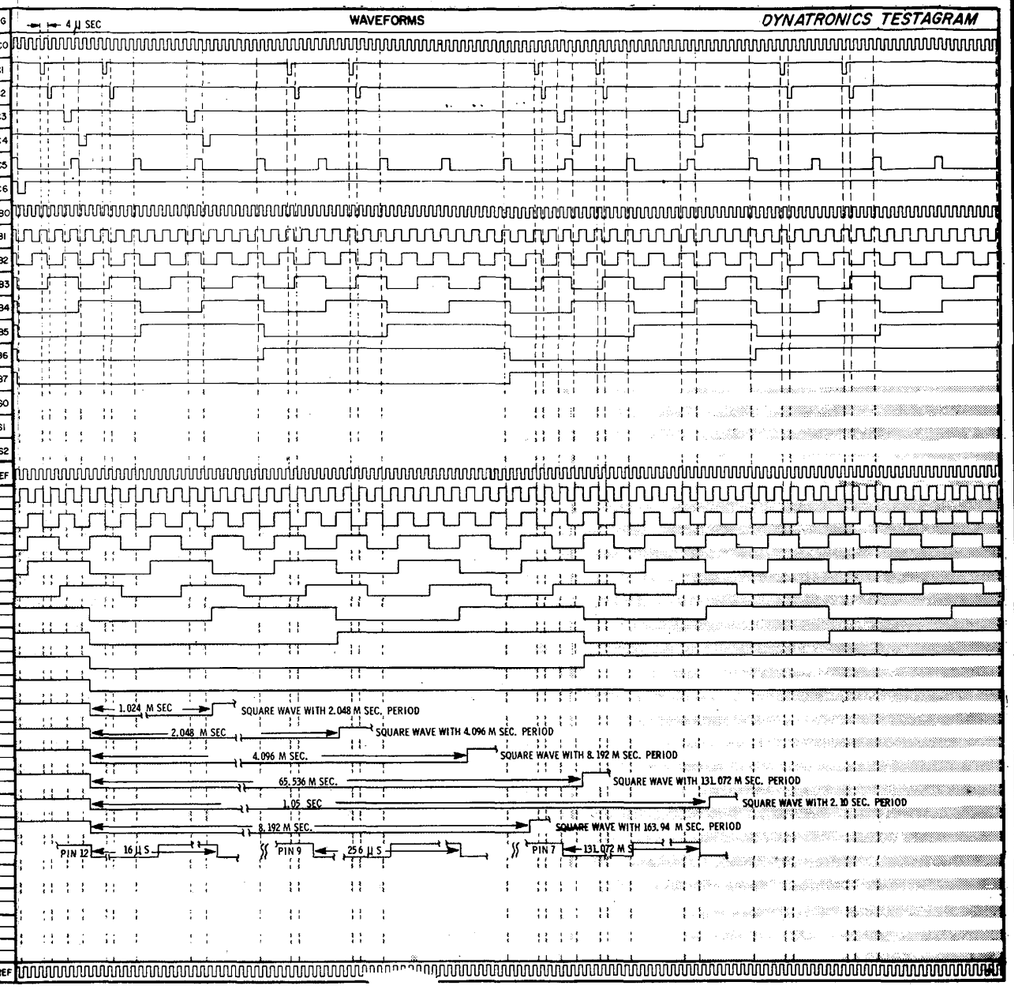


TEST PARAMETERS			
V_{cc}	+5.0V	SIG V	VCC
-V		LOAD REF V	NC
+V		CLK	1 μ sec
-V		BIT CLK	

ROW ASSIGNMENT
10
1
2
3
4
5 GRD
6 +80
7
8
9

INPUT PINS	COL	SIG
	63	+CO
	64	-CI
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
14	70	+BO
	71	+BI
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+SO
	79	+SI
	80	+S2
		+CO REF

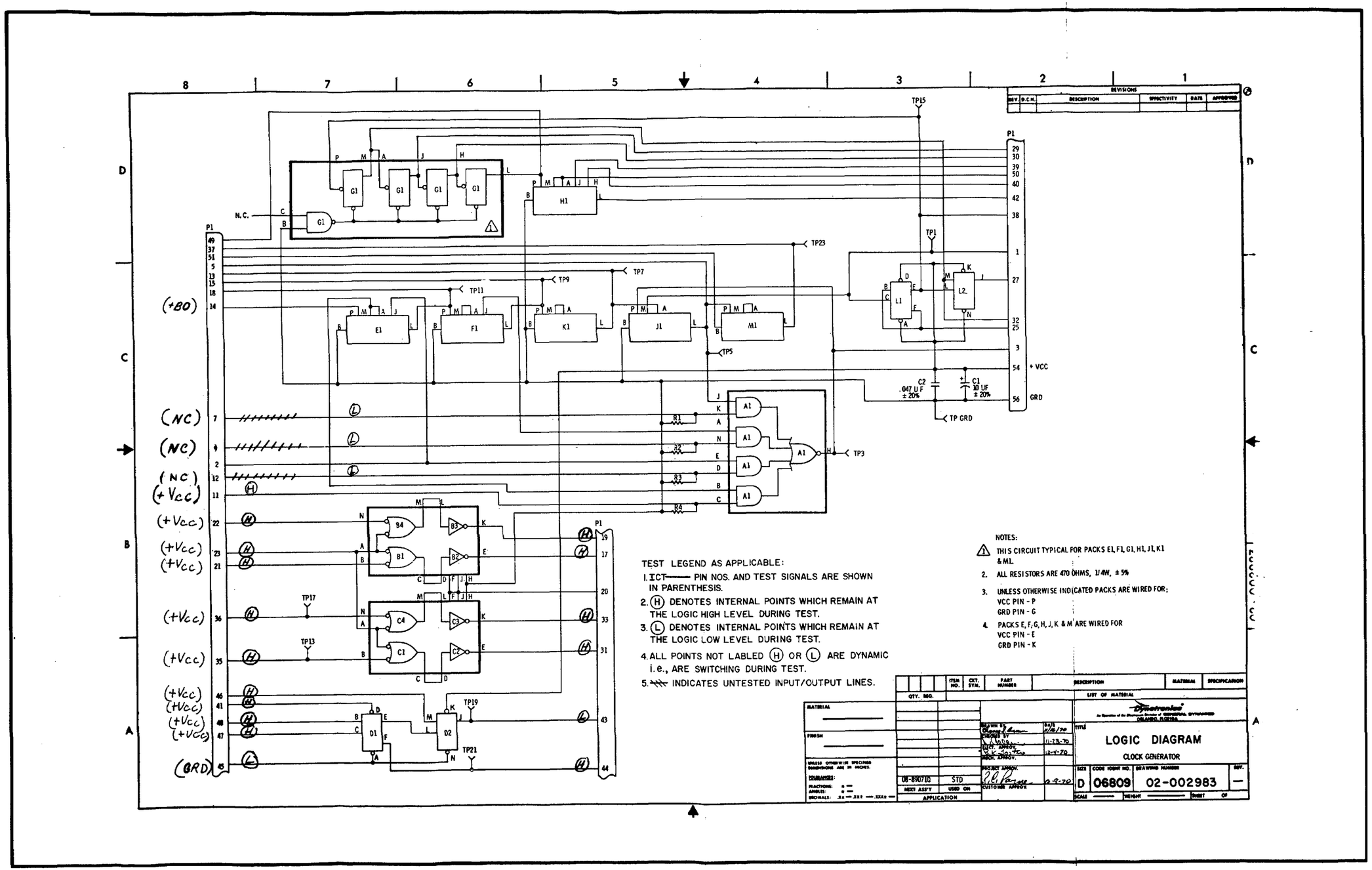
OUTPUT PINS (TEST POINTS)		SWITCH SETTING
3	[3]	
1, 2	[1]	
38, 25*	[15]	
32, 18	[11]	
27		
29		
30		
49		
50, 15	[9]	
39		
40		
42		
5	[5]	
37	[23]	
13	[7]	
3 ▷ (OPTIONAL TEST)	[3]	



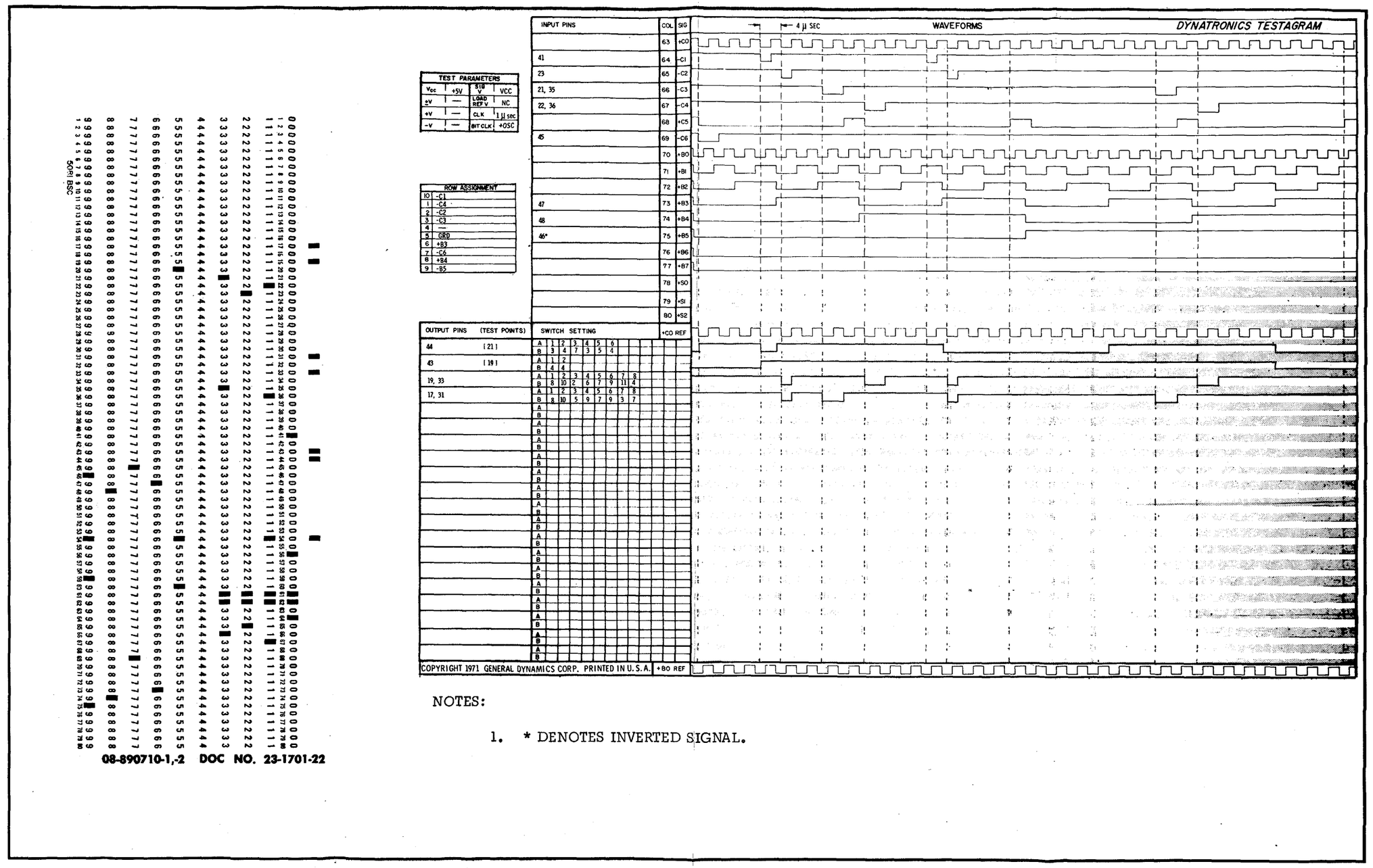
NOTES:

1. THESE OUTPUTS ARE BEYOND THE GO/NO-GO TEST RANGE. USE OSCILLOSCOPE TO CHECK EDGE TIMING.
2. UPON COMPLETION OF ALL TESTING REMOVE POWER FROM THE TEST CARD AND TAPE PIN 11. REPLACE THE CARD, RESTORE POWER AND JUMPER PINS 12,9 AND 7 TO +5V ONE AT A TIME. ON THE SCOPE OBSERVE A SQUAREWAVE WHOSE PERIOD IS SHOWN.
3. * DENOTES INVERTED SIGNAL.

Doc. No. 23-1701-12
P.C. Assembly 08-890710-1
P.C. Logic 02-002983

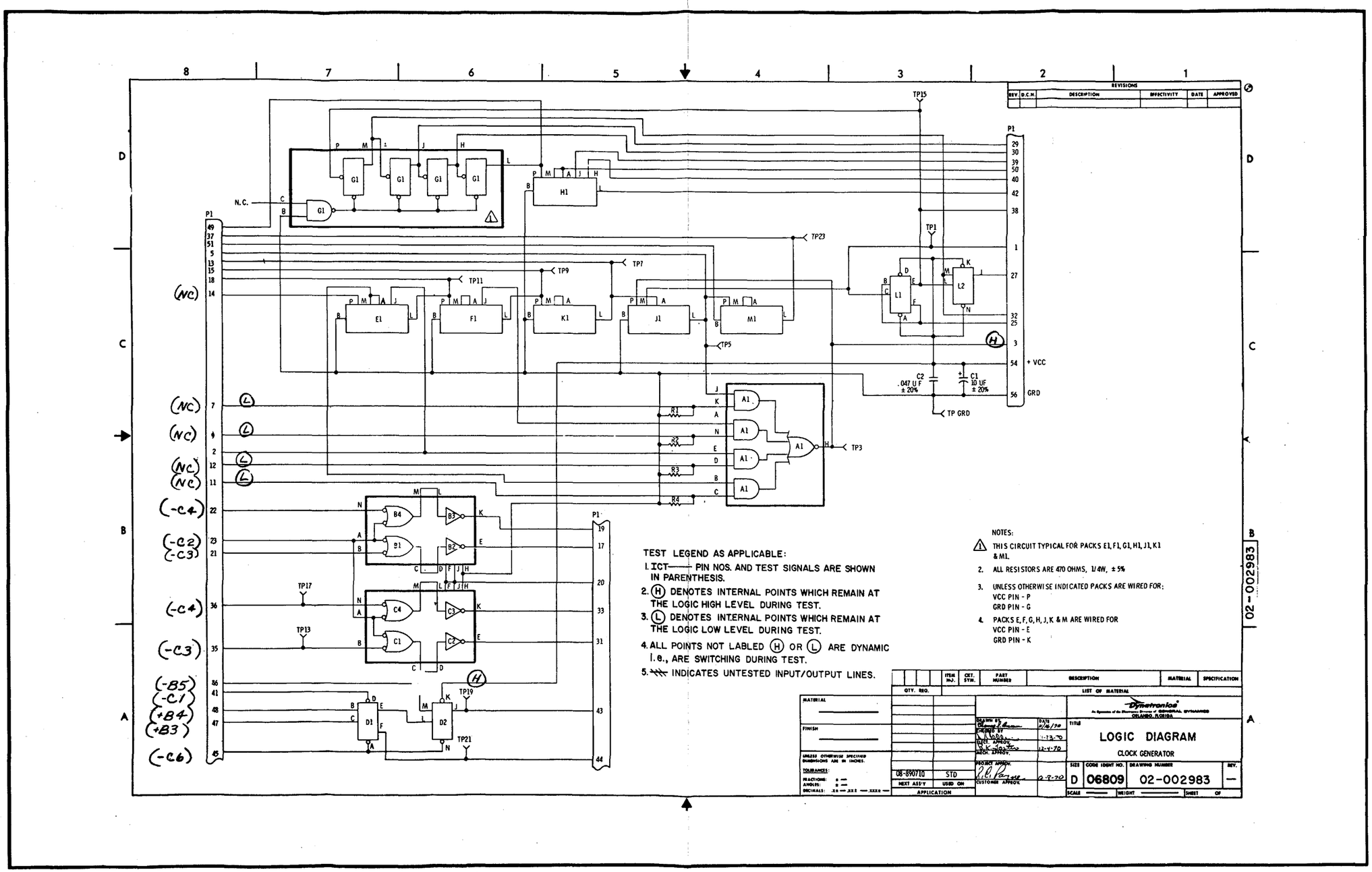


P.C. Assembly 08-890710-1
P.C. Logic 02-002983
Doc. No. 23-1701-12



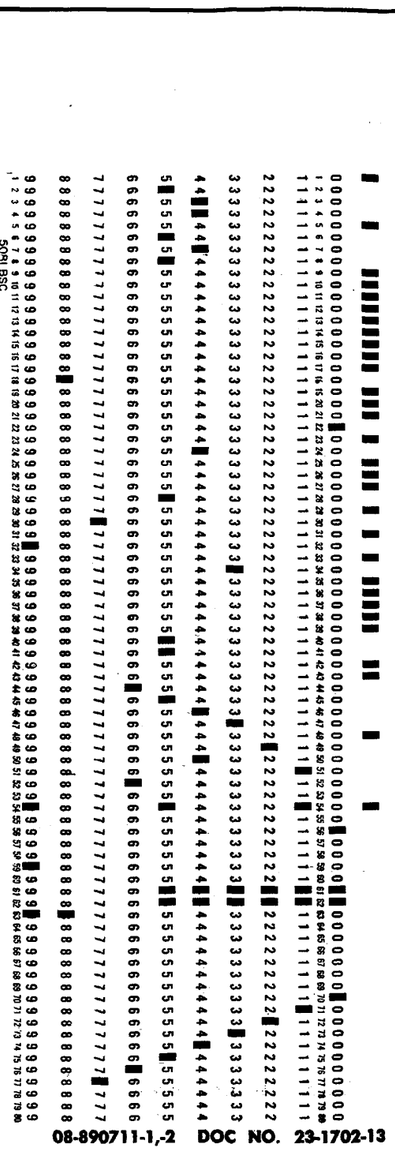
NOTES:

1. * DENOTES INVERTED SIGNAL.



P.C. Assembly 08-890710-1
P.C. Logic 02-002983
Doc. No. 23- 1701-22

9-9/9-10

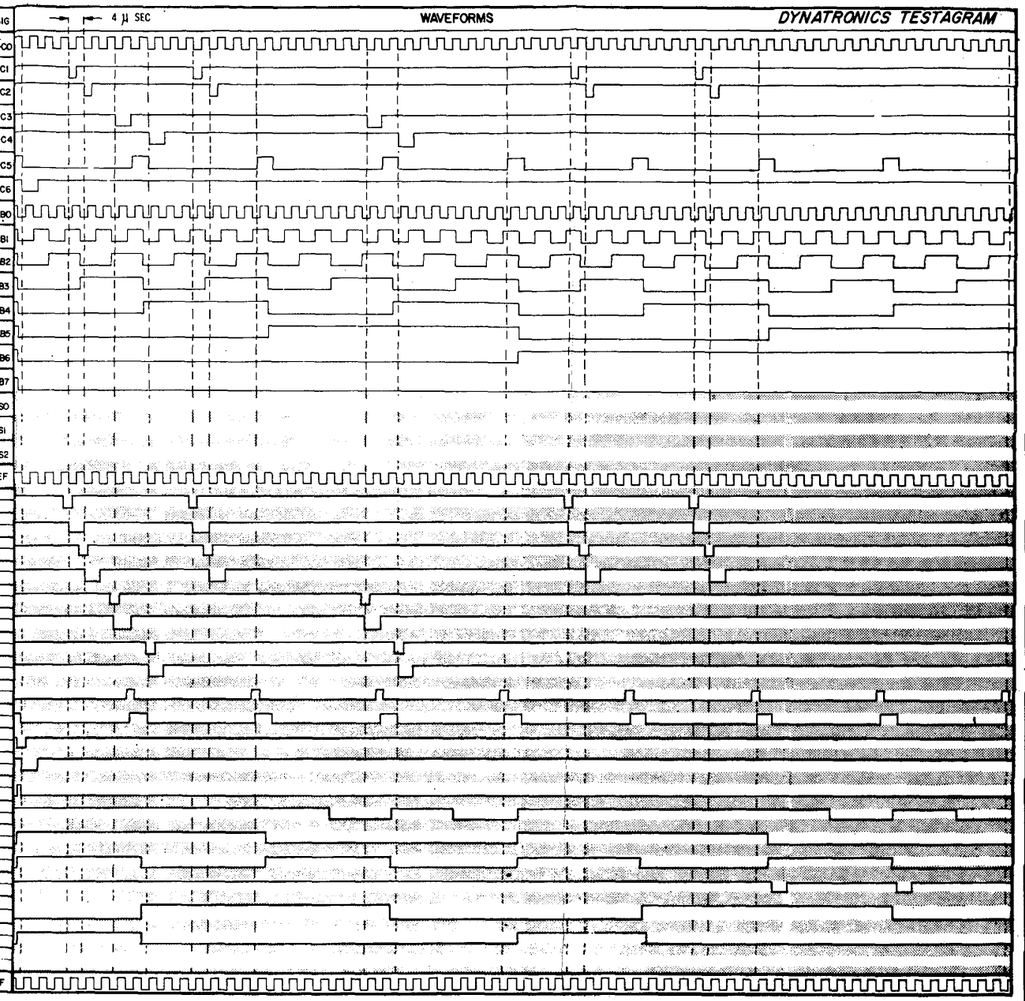


TEST PARAMETERS			
V_{SS}	+5	SIG V	0, +5
±V	—	LOAD REF V	—
+V	—	CLK	1 µS
−V	—	EXT CLK	OSC

ROW ASSIGNMENT	
10	+B0
1	+B1
2	+B2
3	+B3
4	+B4
5	+B5
6	+B6
7	+B7
8	+C0
9	-C0

OUTPUT PINS (TEST POINTS)		SWITCH SETTING
23	(17)	A 1 2 3 4 5 / B 3 5 2 4 10
29		A 1 2 3 4 5 / B 4 8 3 7 11
25	(19)	A 1 2 3 4 5 / B 7 9 6 8 3
26		A 1 2 3 4 5 / B 8 1 7 11 4
11	(11)	A 1 2 3 4 5 / B 4 6 2 4 7
17		A 1 2 3 4 5 / B 5 9 3 7 8
13	(4)	A 1 2 3 4 5 / B 1 3 10 1 4
12		A 1 2 3 4 5 / B 2 6 11 4 5
15	(24)	A 1 2 3 / B 8 10 7
14		A 1 2 3 / B 3 9 2
10	(2)	A 1 2 3 / B 2 4 #
16		A 1 2 3 / B 3 7 #
36, 19*, 20*	(6*)	A 1 2 3 / B 2 3 #
43		A 1 2 3 4 / B 2 5 10 4
38	(13)	A 1 2 3 / B 2 11 9
21	(9)	A 1 2 3 / B 2 1 11
42	(15)	A 1 2 3 / B 8 1 7
9, 1, 5	(1, 3, 5)	A 1 2 3 / B 1 10 8
48		A 1 2 3 / B 2 1 9
		A / B

INPUT PINS	COL	SIG
18, 32*	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
22	70	+B0
51	71	+B1
49	72	+B2
47, 34	73	+B3
24, 50, 4, 3, 7, 46	74	+B4
2, 6, 45, 8, 41, 28, 40	75	+B5
44, 52	76	+B6
30	77	+B7
	78	+S0
	79	+S1
	80	+S2
		+C0 REF



NOTES:

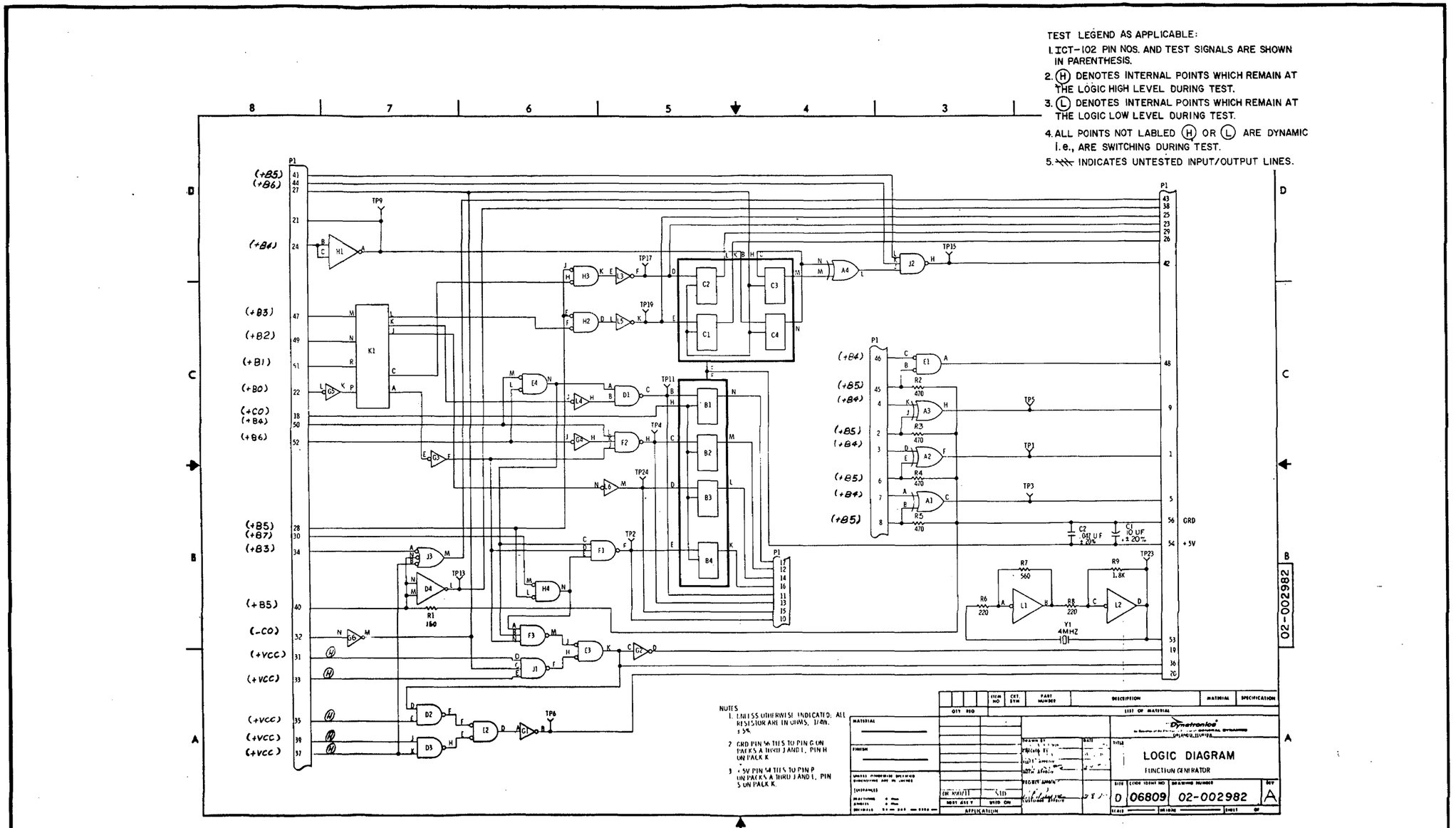
1. * DENOTES INVERTED SIGNAL

2. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH NO. 12 WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.

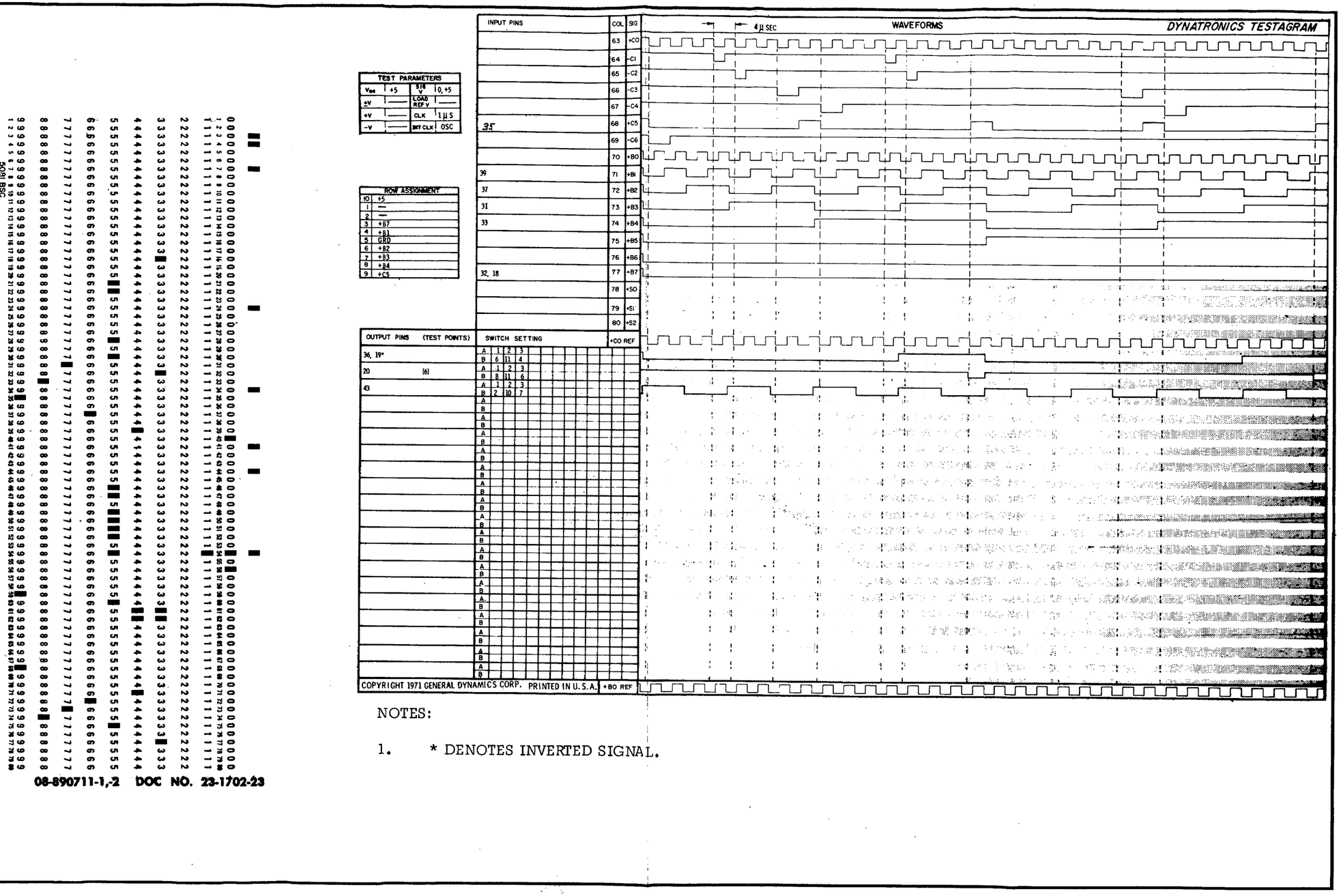
P.C. Assembly 08-890711
Doc. No. 23-1702-13
P.C. Logic 02-002982

9-11/9-12



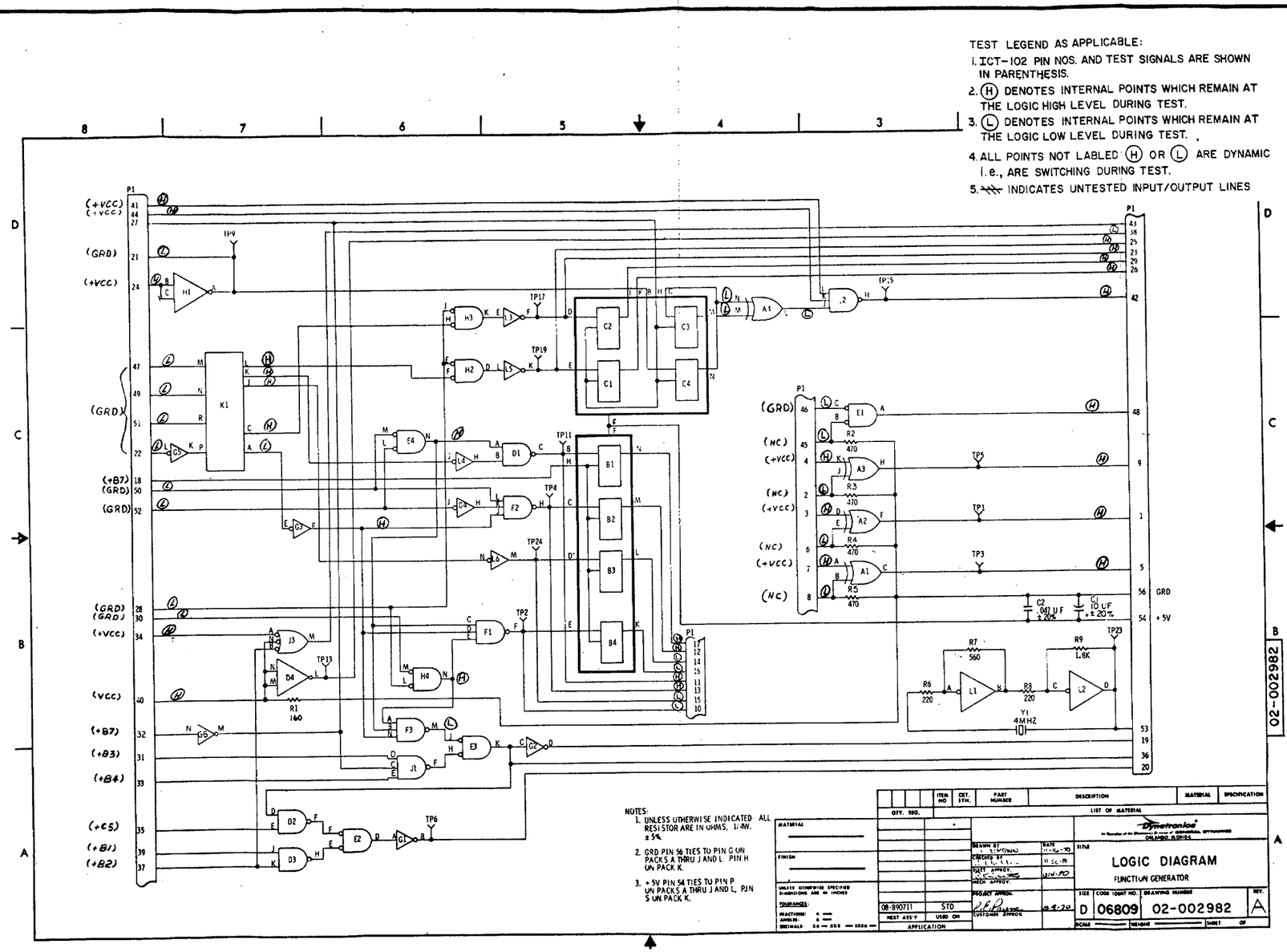
P.C. Assembly 08-890711
P.C, Logic 02-002982
Doc. No. 1702-13

9-13/9-14



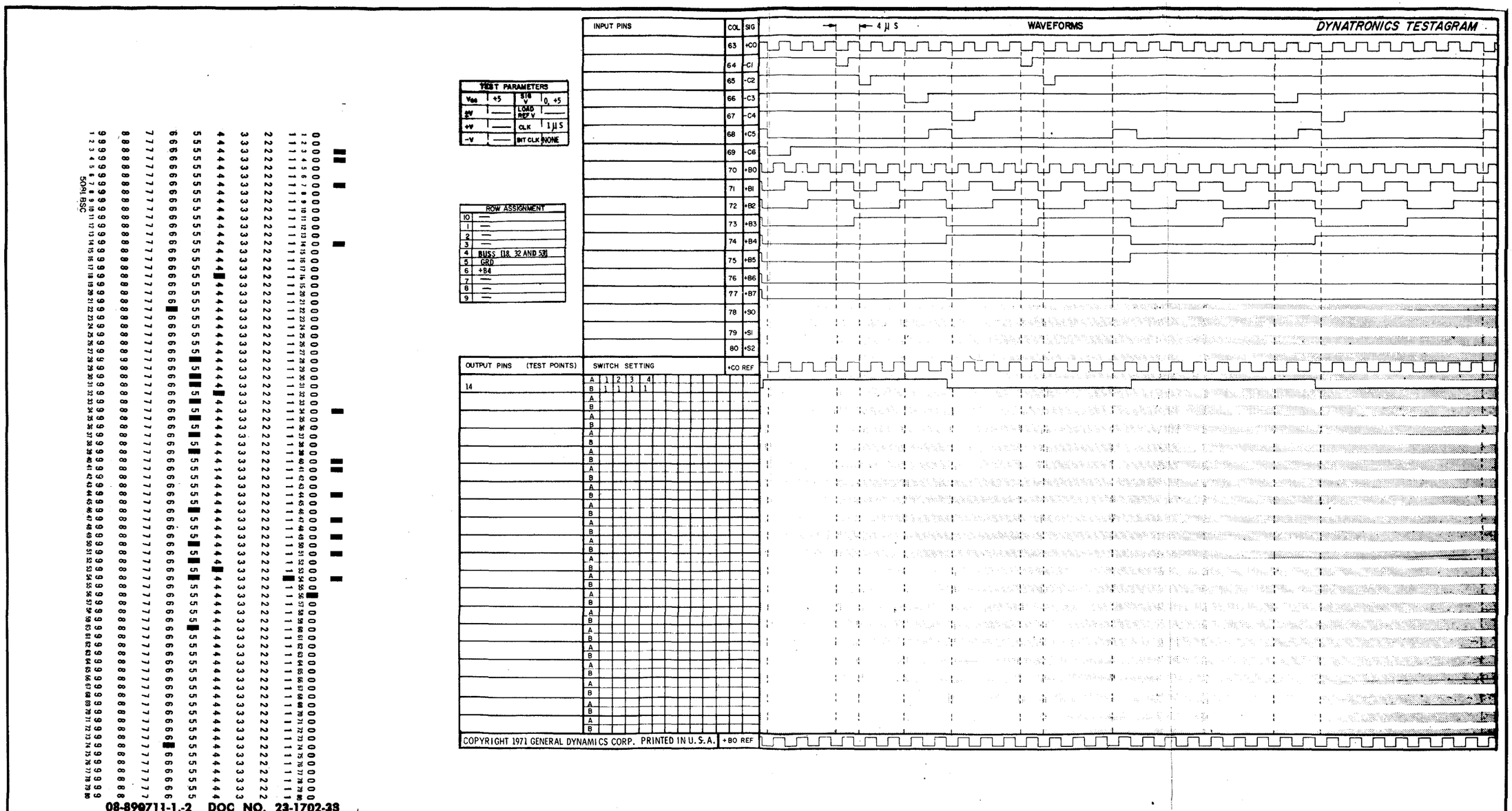
NOTES:

1. * DENOTES INVERTED SIGNAL.



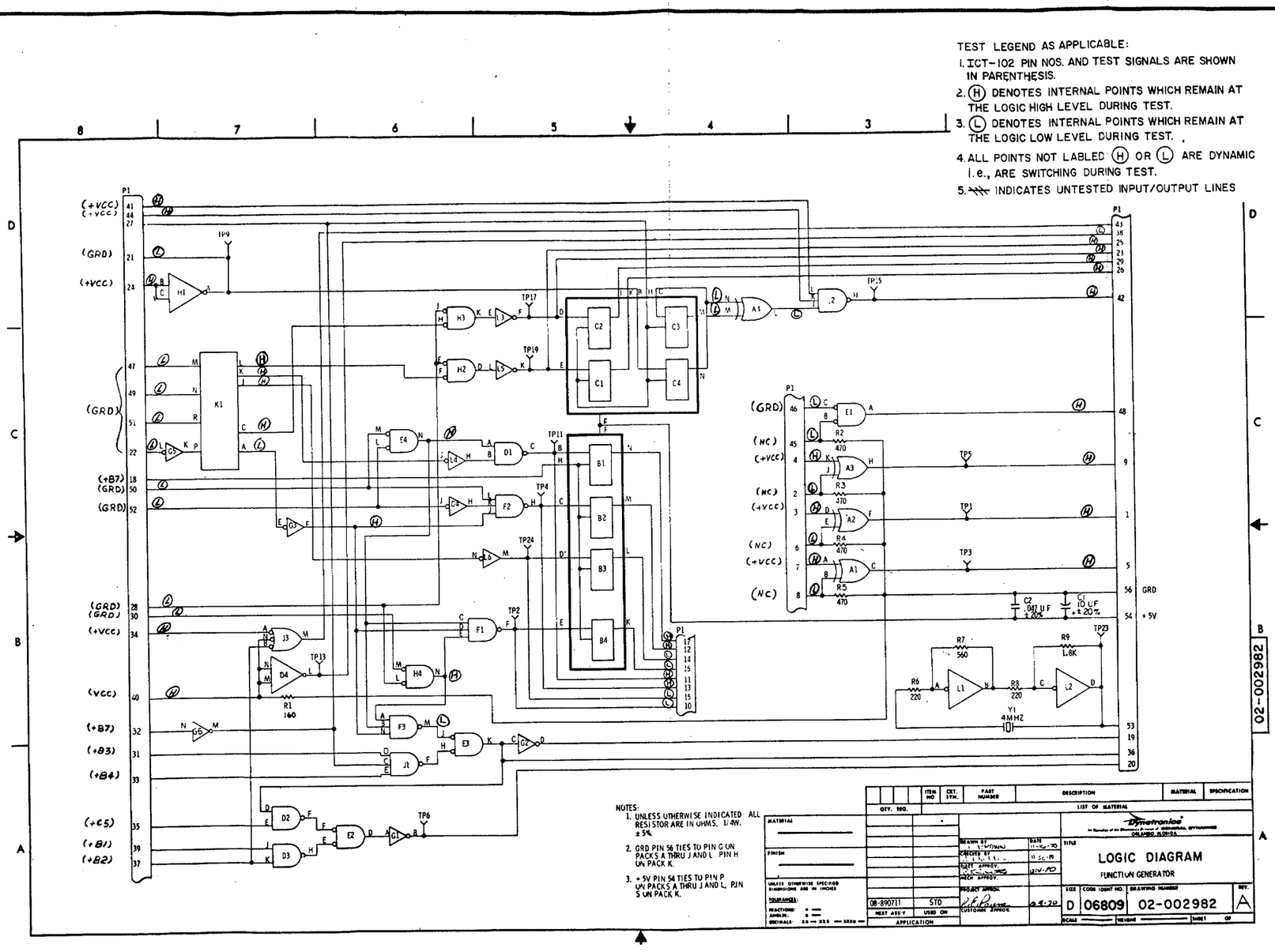
P.C. Assembly 08-890711
P.C. Logic 02-002982
Doc. No. 1702-23

9-17/9-18



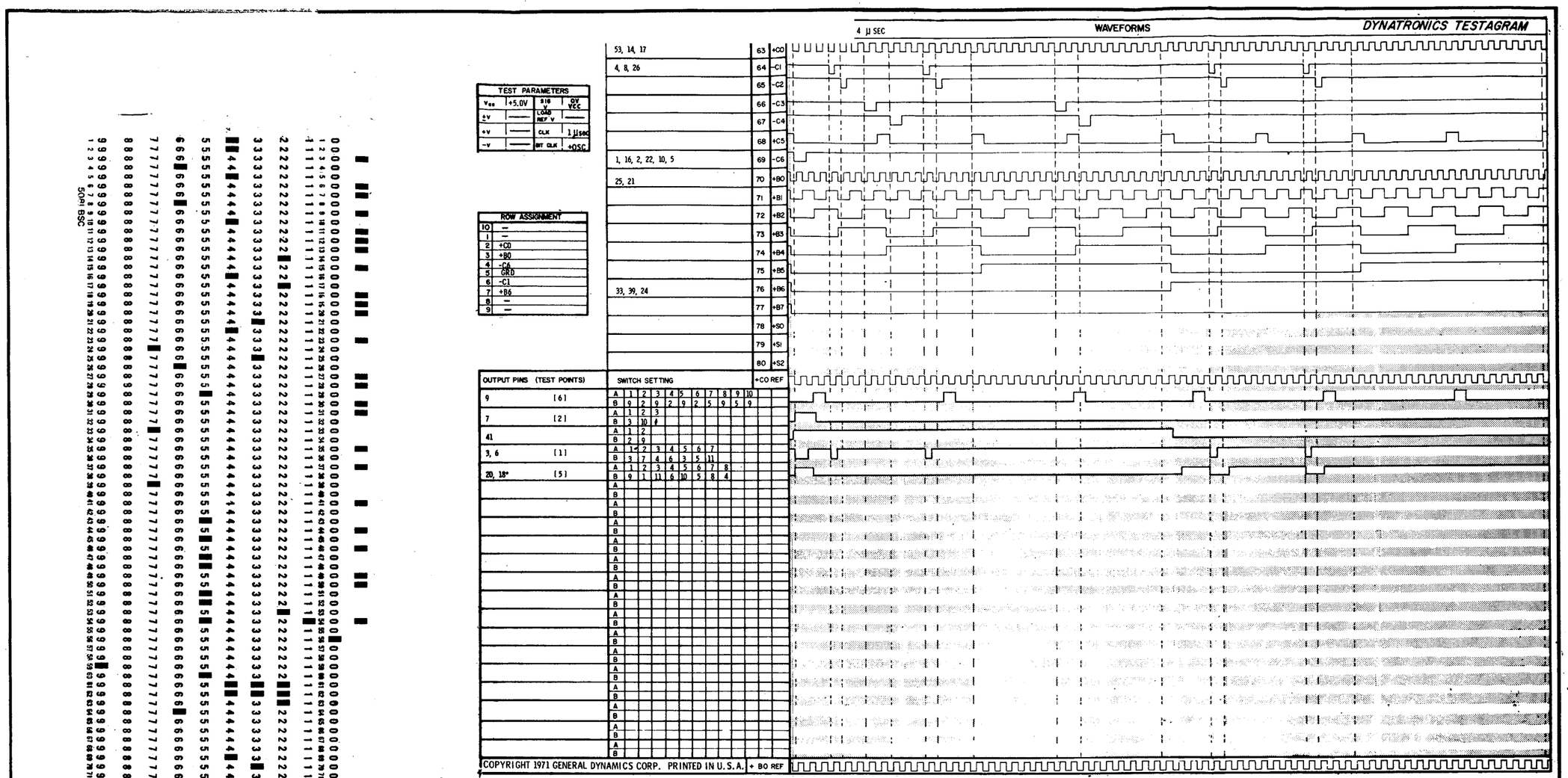
Doc. No. 23-1702-33
P.C, Assembly 08-890711
P.C. Logic 02-002982

9-19/9-20



P.C. Assembly 08-890711
Doc. No. -1702-33
P.C. Logic 02-002982

9-21/9-22

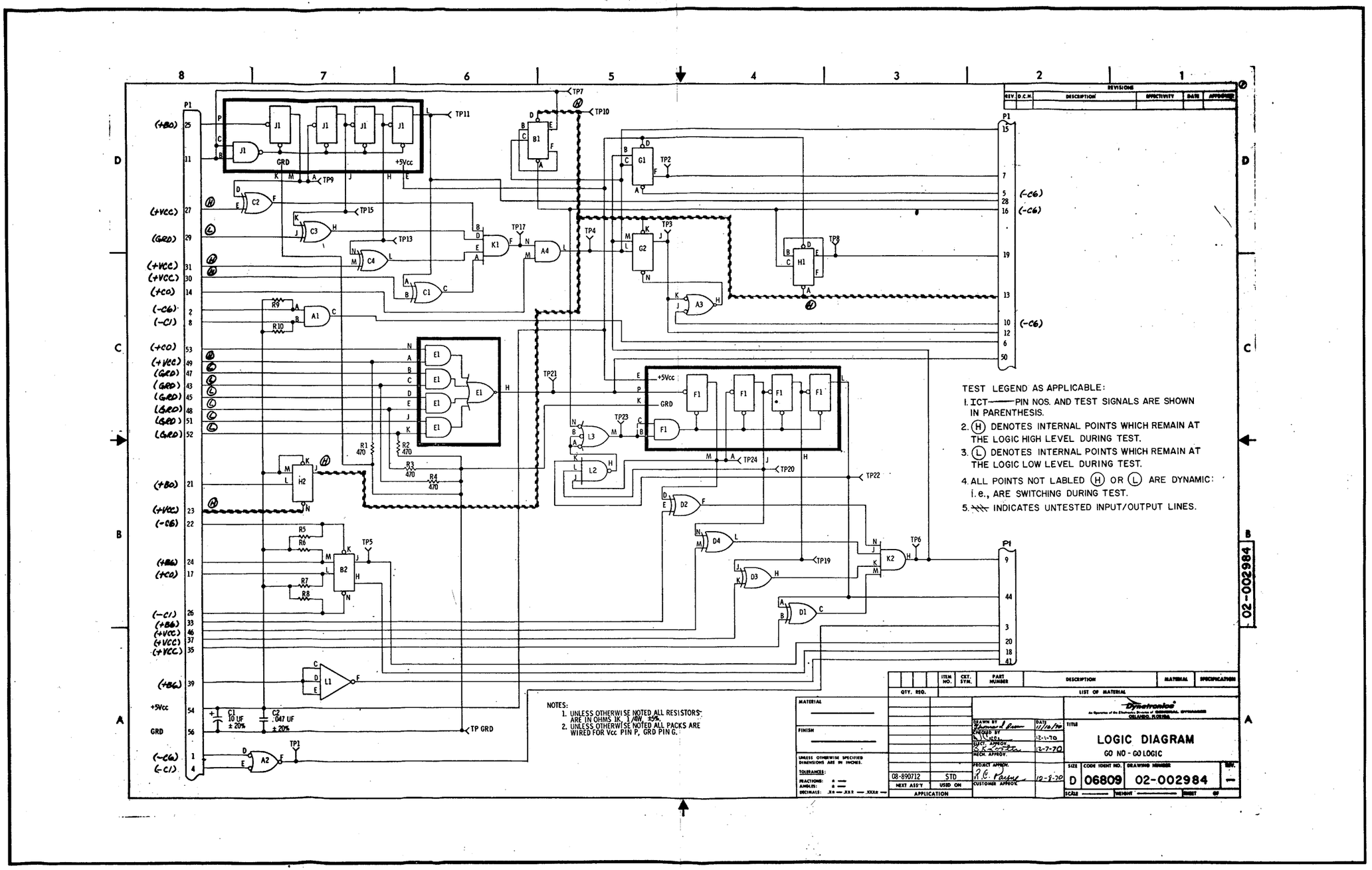


NOTES:

1. * DENOTES INVERTED SIGNAL.
2. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

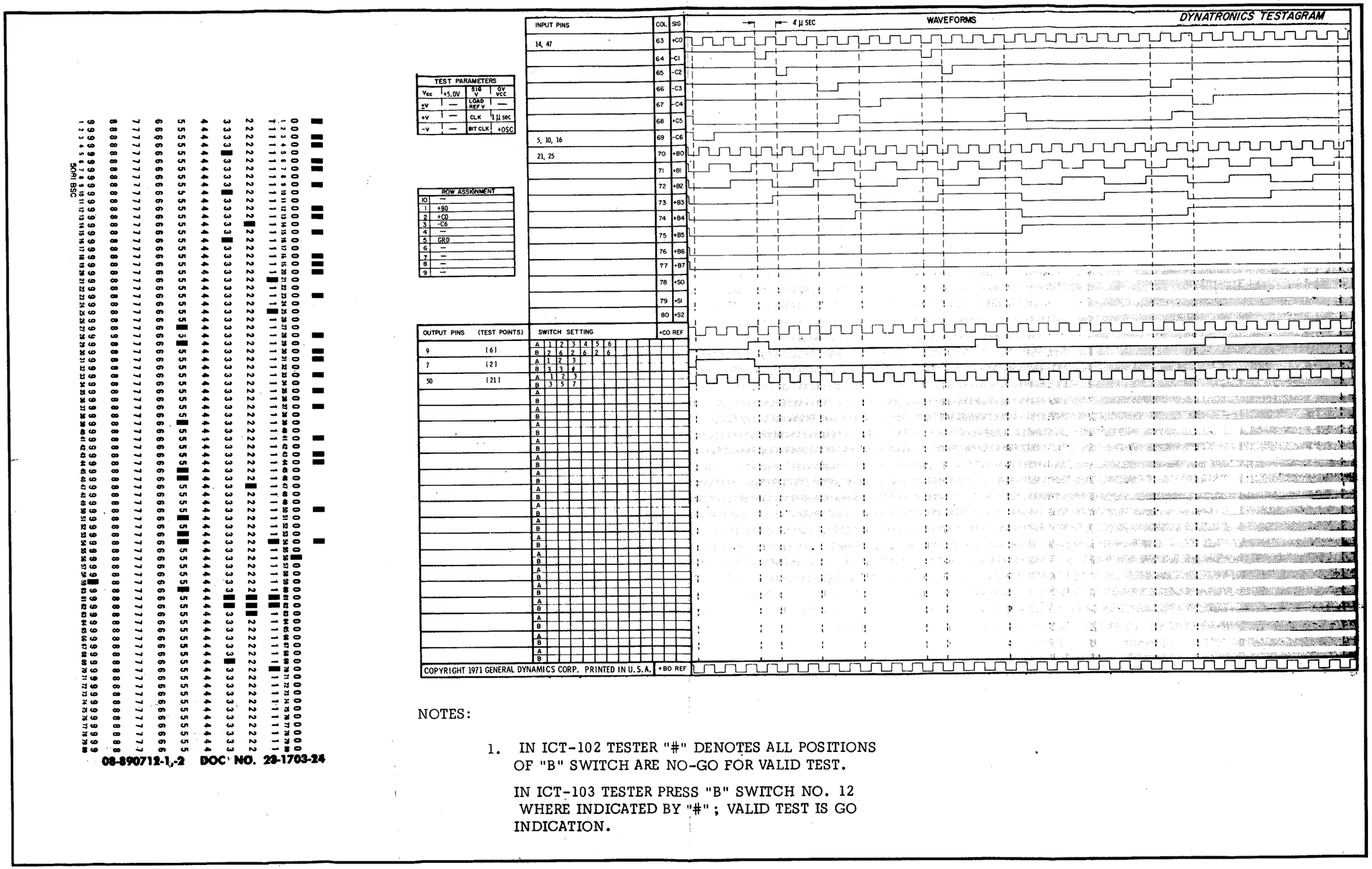
   IN ICT-103 TESTER PRESS "B" SWITCH NO. 12 WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.

P.C. Assembly 08-890712-1
P.C. Logic 02-002984
Doc. No. 23- 1703-14



P.C. Assembly 08-890712-1
Doc. No. 23-1703-24
P.C. Logic 02-002984

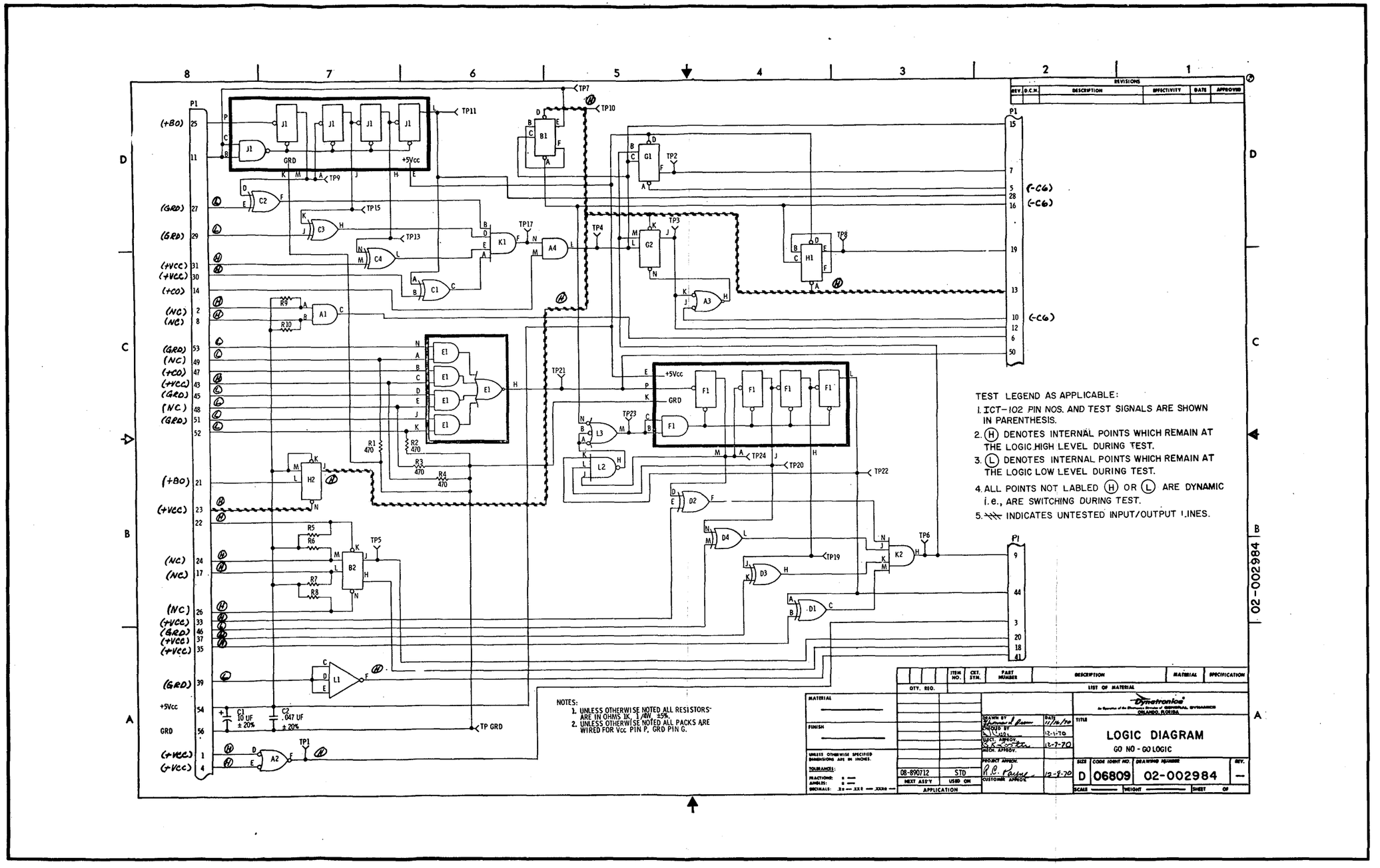
9-25/9-26



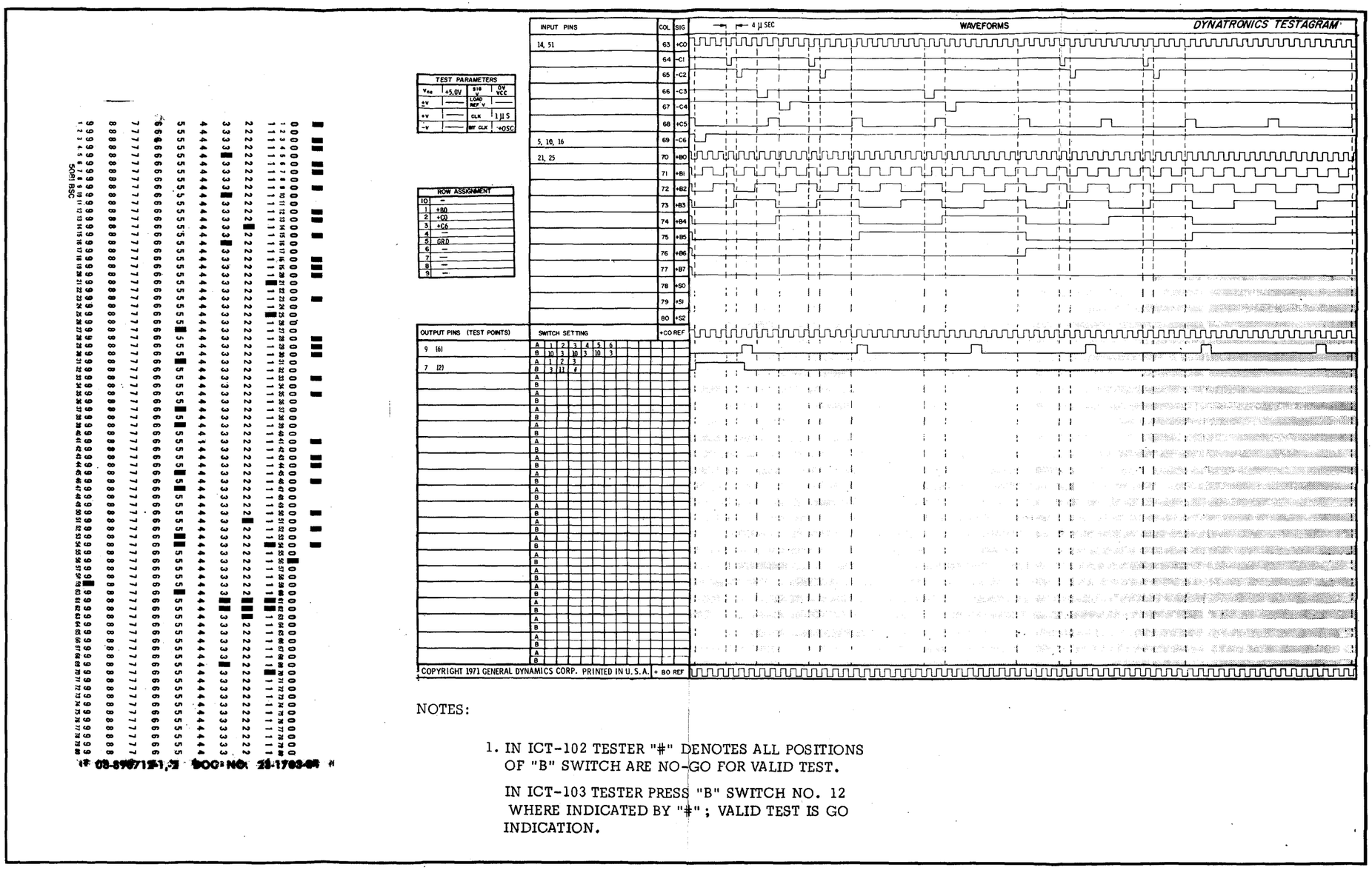
NOTES:

1. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH NO. 12 WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.



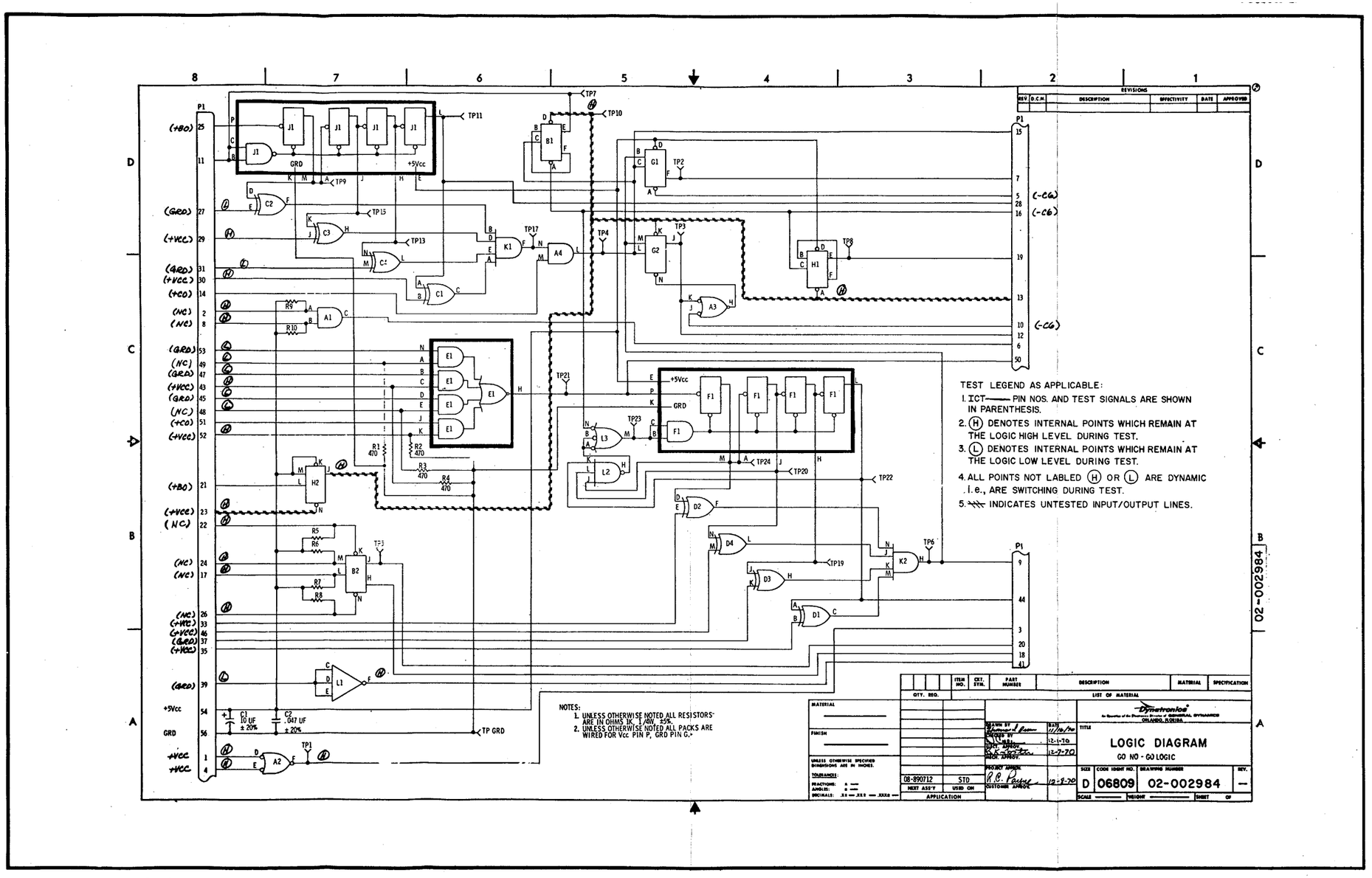
P.C. Assembly 08-890712-1
P.C. Logic 02-002982
Doc. No. 23-1702-24



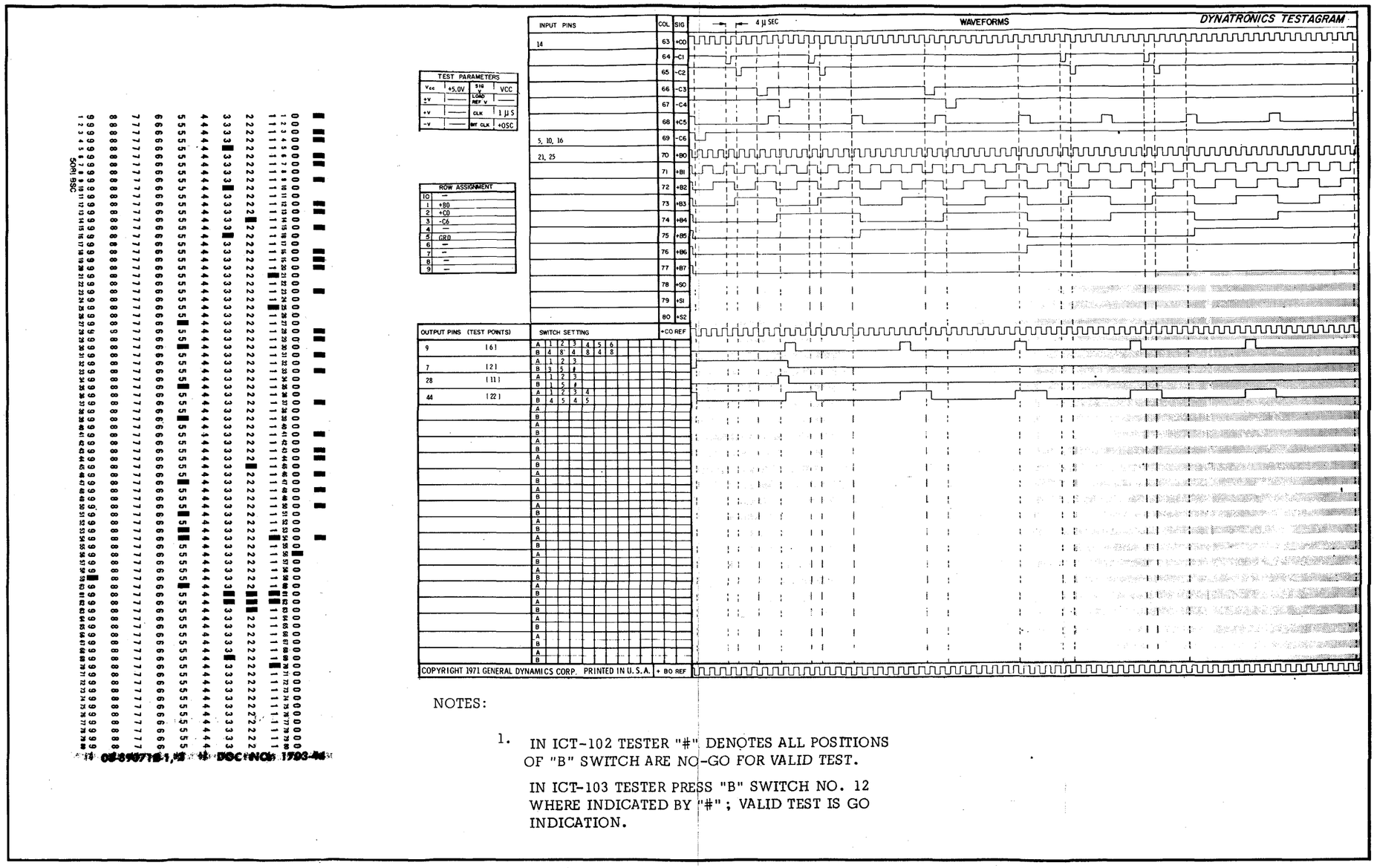
NOTES:

1. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH NO. 12 WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.



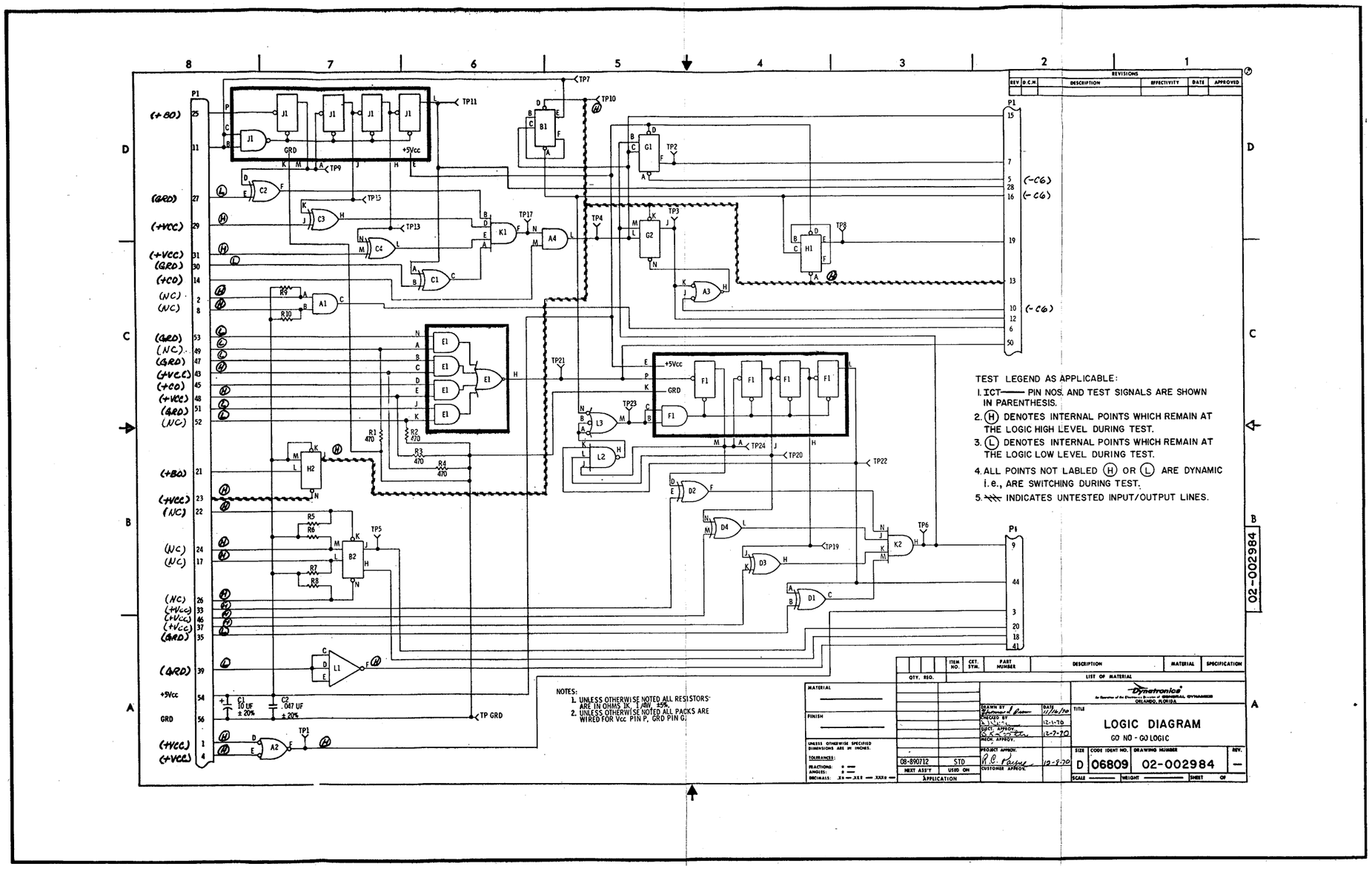
P.C. Assembly 08-890712-1
P.C. Logic 02-002984

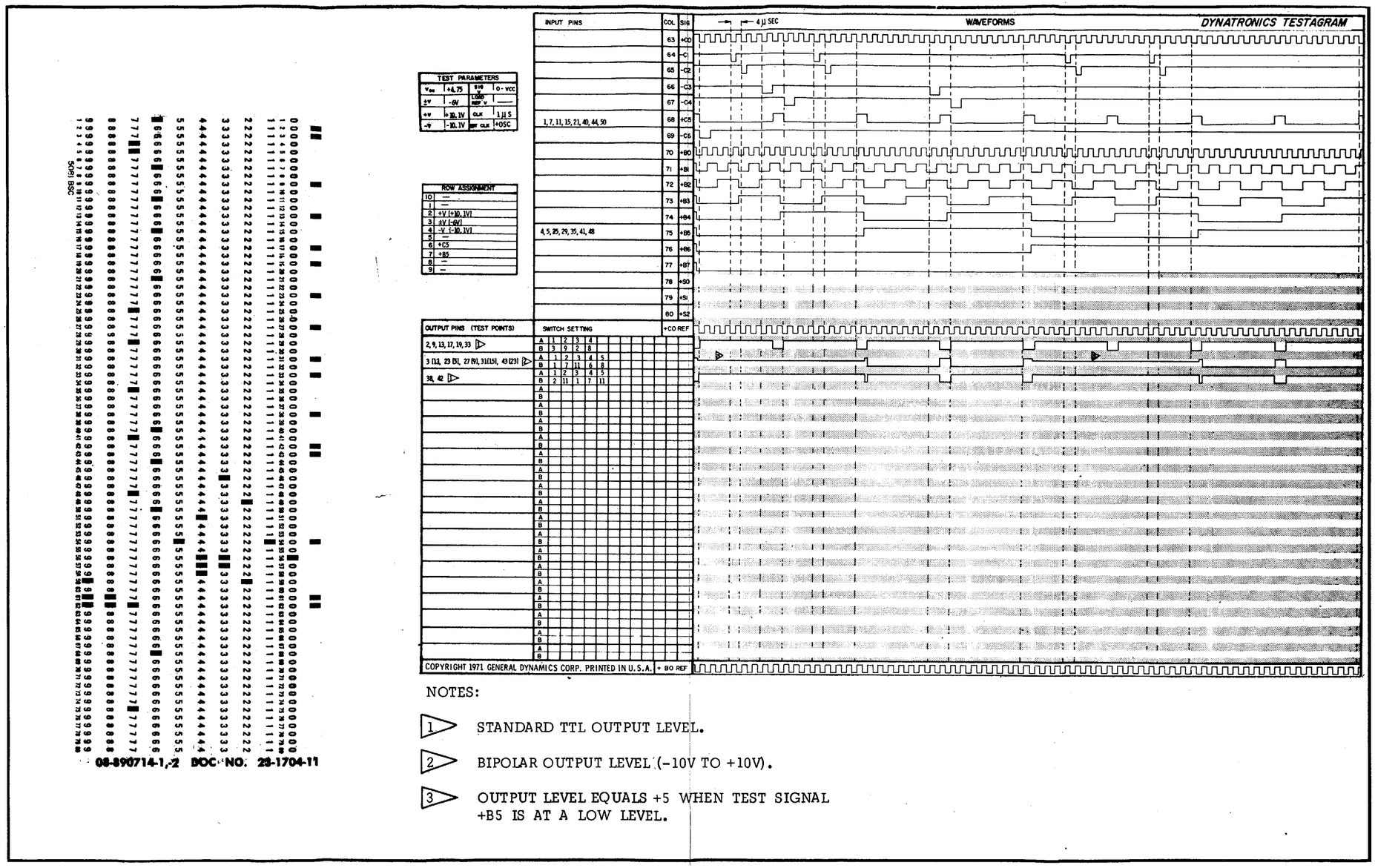


NOTES:

1. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

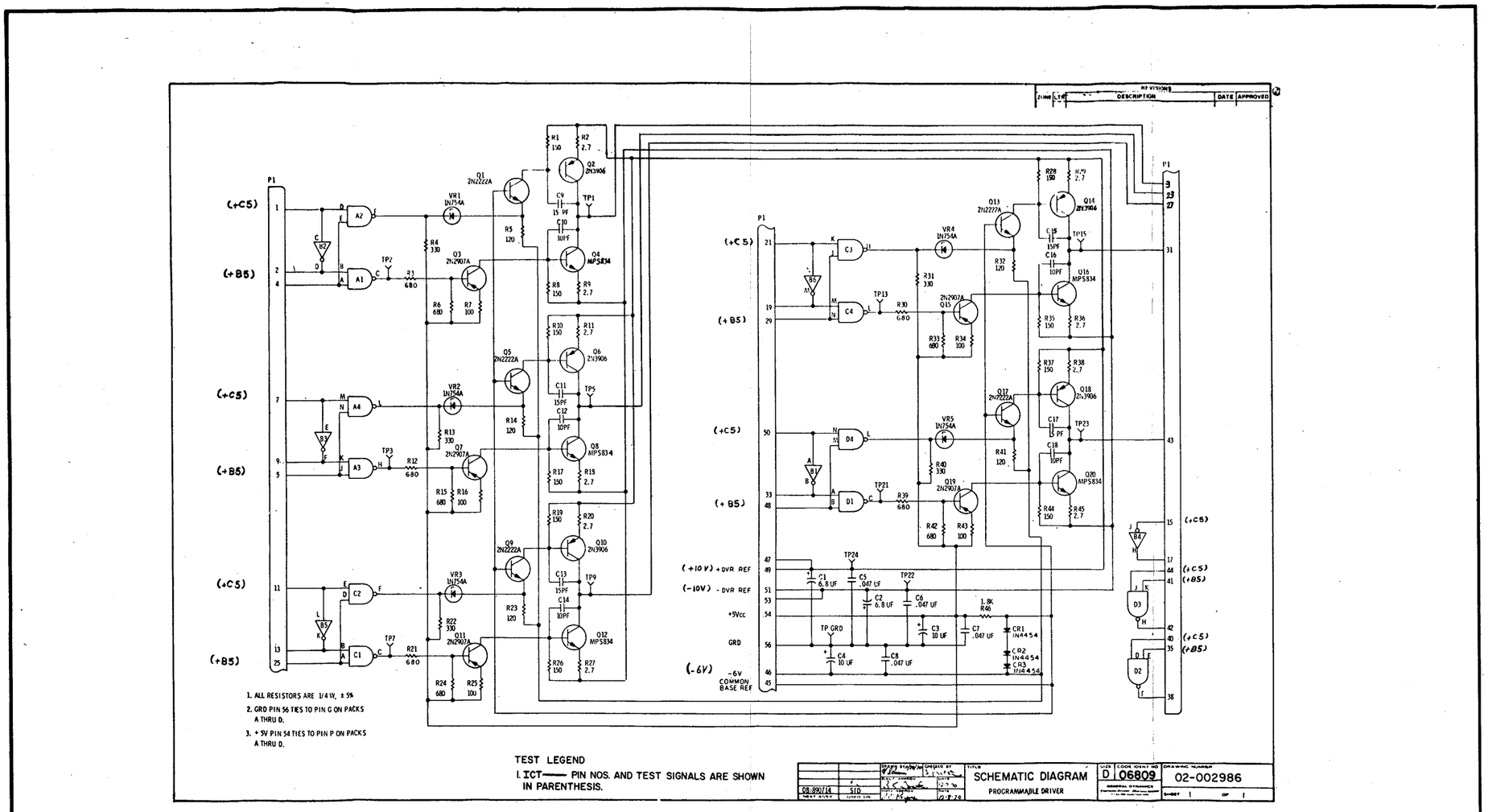
   IN ICT-103 TESTER PRESS "B" SWITCH NO. 12 WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.


TEST LEGEND AS APPLICABLE:
1. ICT—— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. INDICATES UNTESTED INPUT/OUTPUT LINES.
NOTES:
1. UNLESS OTHERWISE NOTED ALL RESISTORS ARE IN OHMS 1K, 1/4W, 5%.
2. UNLESS OTHERWISE NOTED ALL PACKS ARE WIRED FOR Vcc PIN P, GRD PIN G.
REVISIONS
REV D.C.N. DESCRIPTION EFFECTIVITY DATE APPROVED
LIST OF MATERIAL
ITEM NO. CKT. SYM. PART NUMBER DESCRIPTION MATERIAL SPECIFICATION QTY. REQ.
Dynetronics
ORLANDO, FLORIDA
TITLE
LOGIC DIAGRAM
GO NO - GO LOGIC
SIZE D CODE IDENT NO. 06809 DRAWING NUMBER 02-002984 REV. —
SCALE — WEIGHT — SHEET OF
08-890712 STD
NEXT ASS'Y USED ON
APPLICATION
02-002984

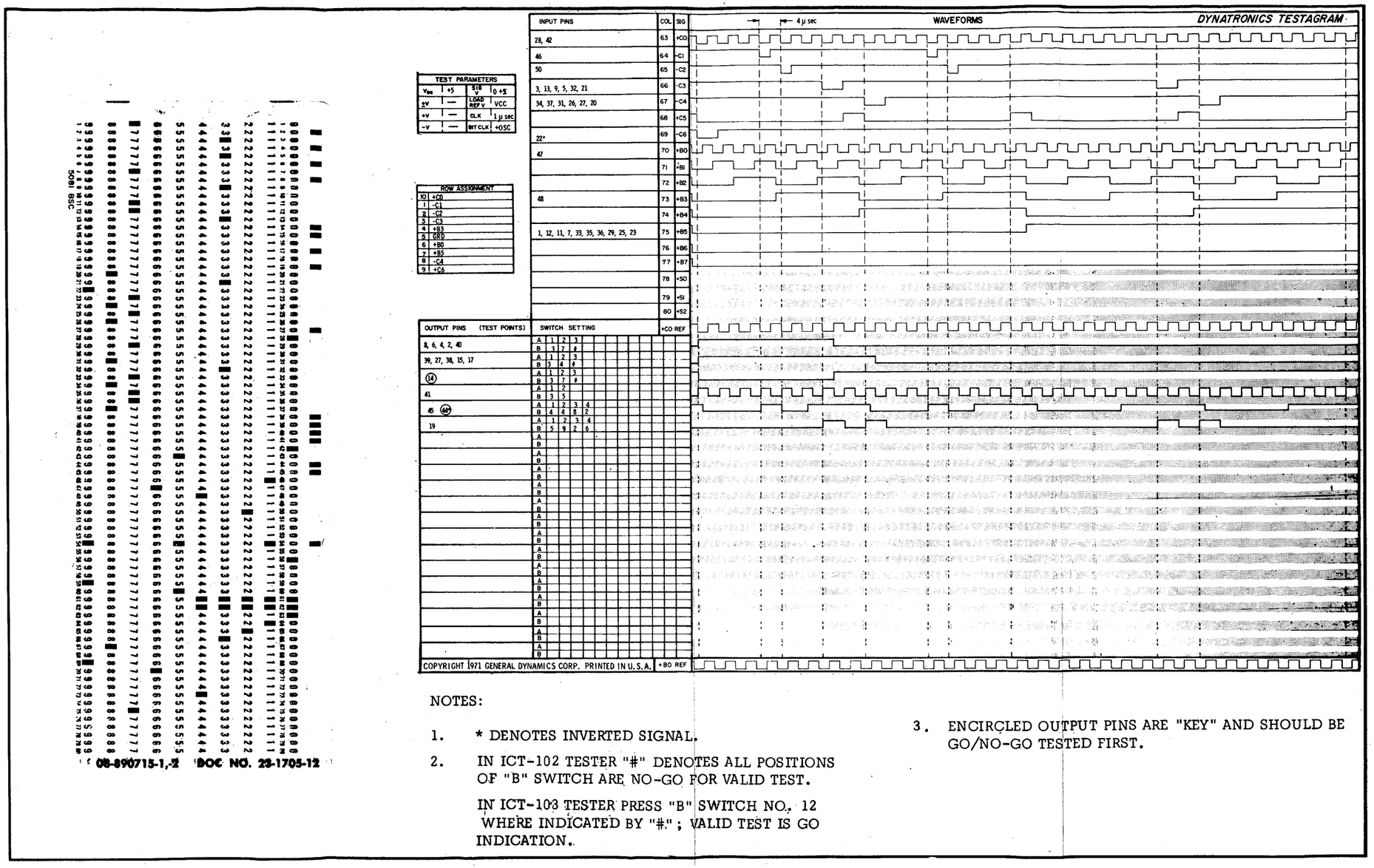


NOTES:

1. STANDARD TTL OUTPUT LEVEL.
2. BIPOLAR OUTPUT LEVEL (-10V TO +10V).
3. OUTPUT LEVEL EQUALS +5 WHEN TEST SIGNAL +B5 IS AT A LOW LEVEL.



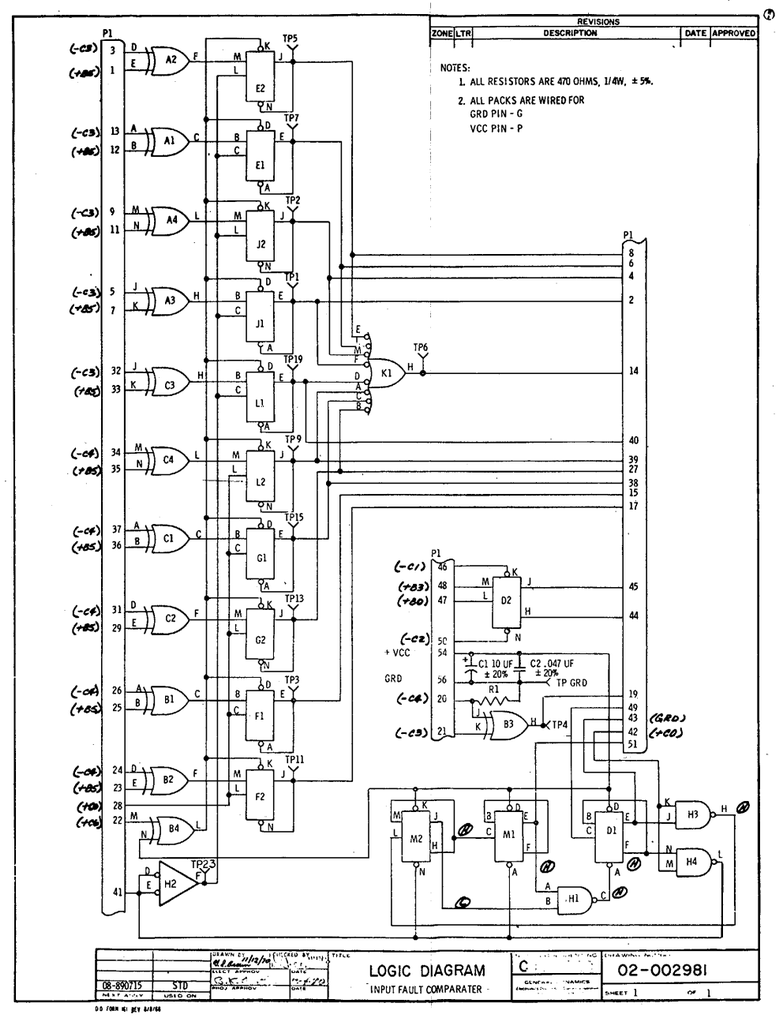
P.C. Assembly 08-890714
P.C. Logic 02-002986



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

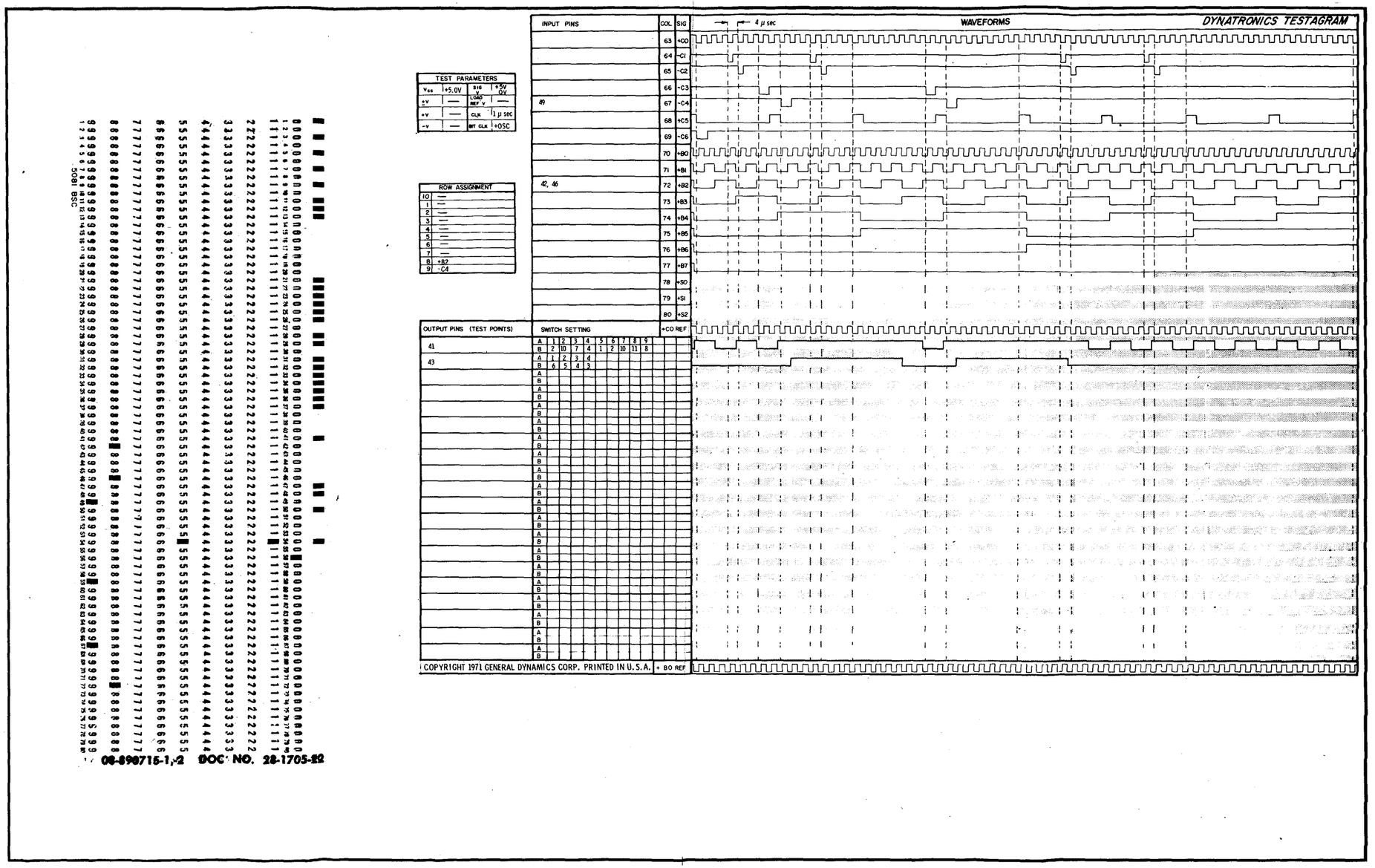
   IN ICT-103 TESTER PRESS "B" SWITCH NO. 12 WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

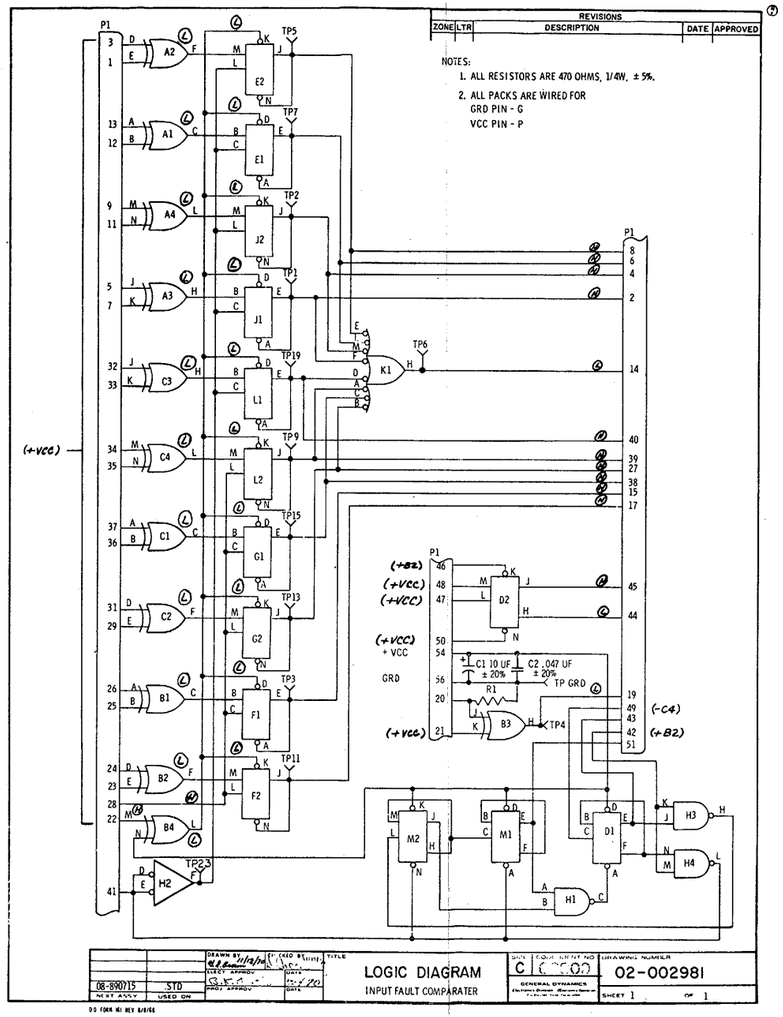


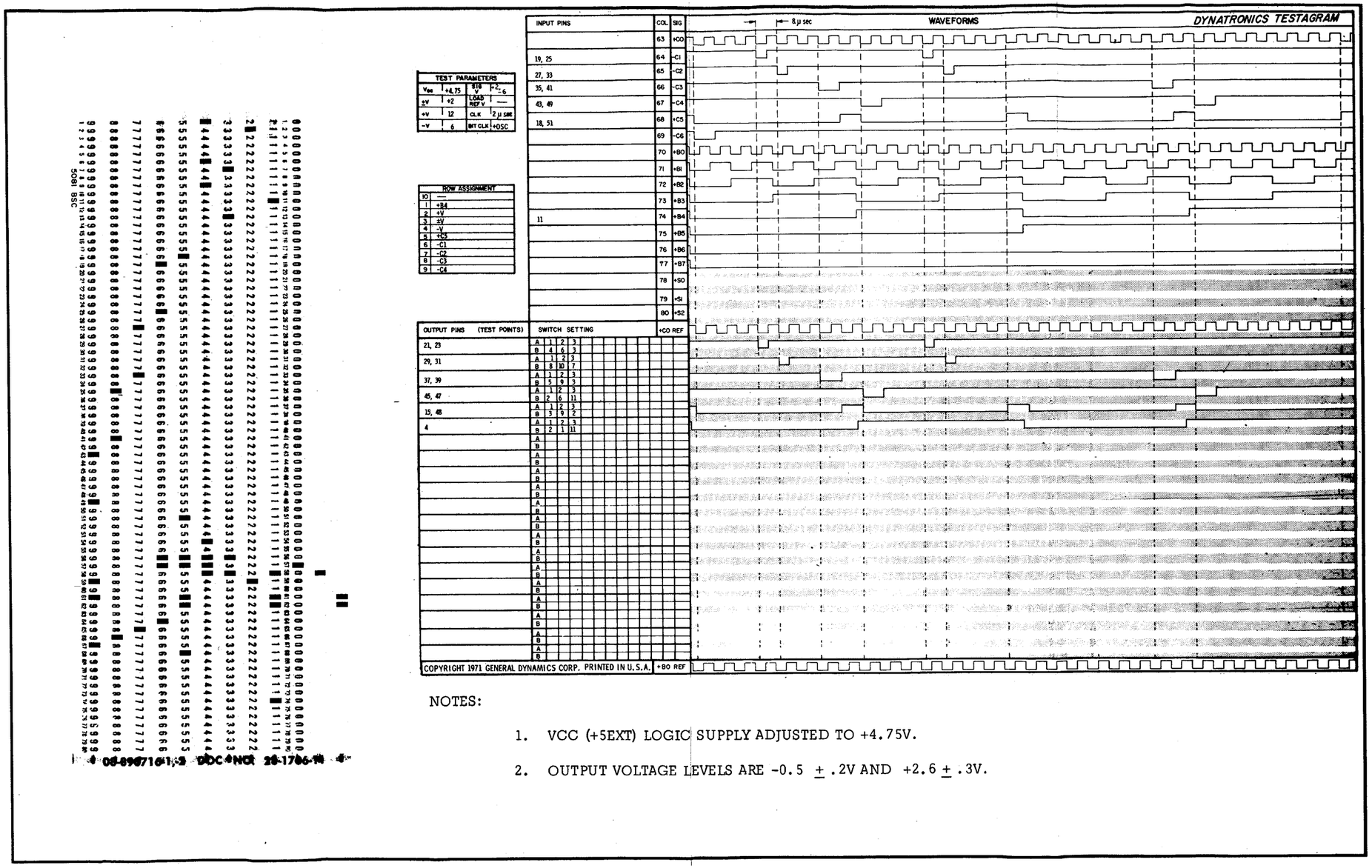
TEST LEGEND AS APPLICABLE:

1. ICT—— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I.e., ARE SWITCHING DURING TEST.
5. ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES.

P.C. Assembly 08-890715
P.C. Logic 02-002981

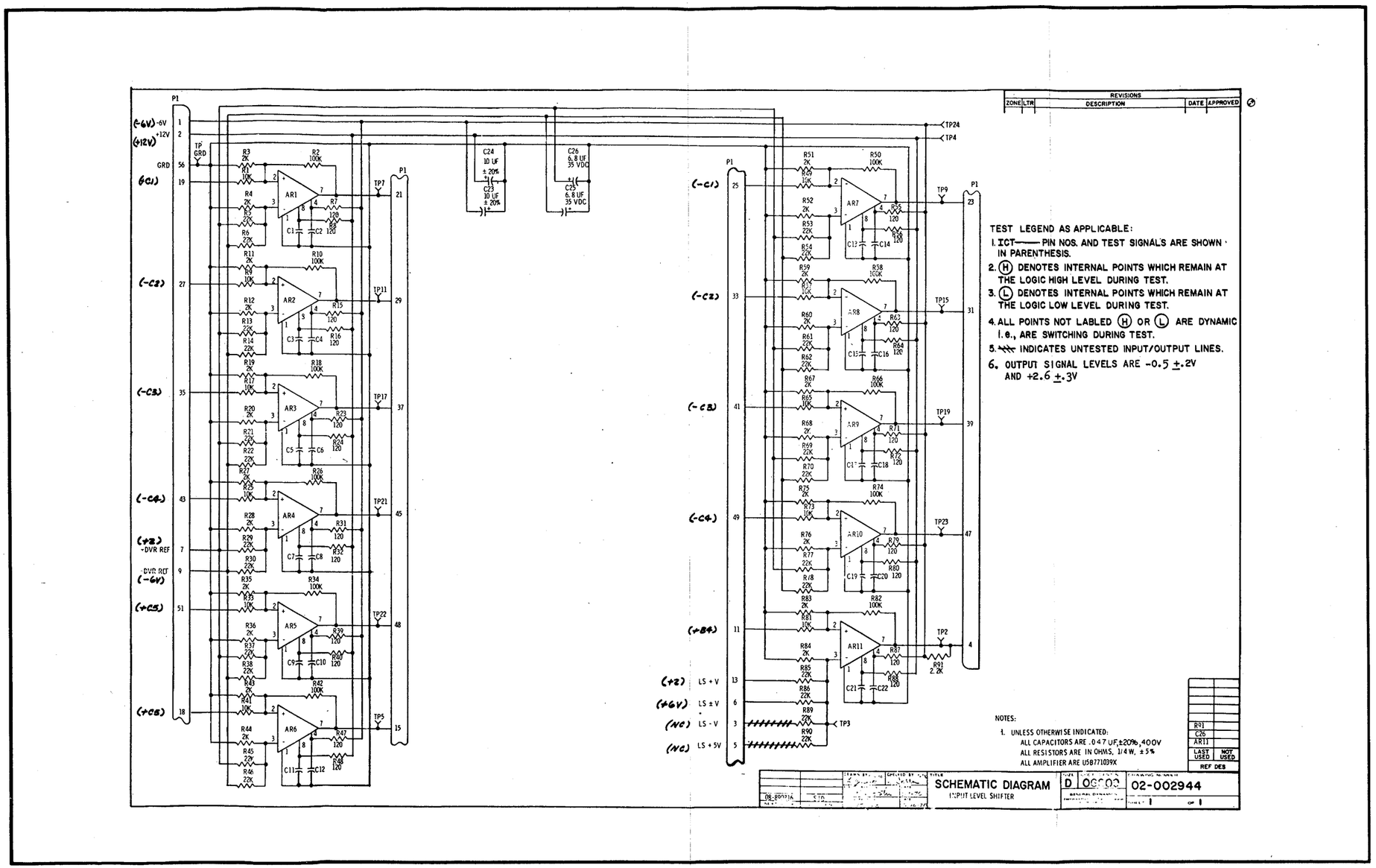

TEST PARAMETERS
ROW ASSIGNMENT
INPUT PINS
OUTPUT PINS (TEST POINTS)
SWITCH SETTING
WAVEFORMS
4 μ sec
DYNATRONICS TESTAGRAM
COPYRIGHT 1971 GENERAL DYNAMICS CORP. PRINTED IN U.S.A.
08-890715-1,-2
DOC NO. 28-1705-22


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
NOTES:
1. ALL RESISTORS ARE 470 OHMS, 1/4W, ± 5%.
2. ALL PACKS ARE WIRED FOR
GRD PIN - G
VCC PIN - P
TEST LEGEND AS APPLICABLE:
1. ICT——PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES.
(+VCC)
C1 10 UF ± 20%
C2 .047 UF ± 20%
R1
TP GRD
(-C4)
(+B2)
LOGIC DIAGRAM
INPUT FAULT COMPARATER
08-890715
STD
02-002981
SHEET 1 OF 1



NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. OUTPUT VOLTAGE LEVELS ARE -0.5 ± .2V AND +2.6 ± .3V.



P.C. Assembly 08-890716
P.C. Logic 02-002944

APPENDIX A

TOPIC INDEX

APPENDIX A (CONT'D)

APPENDIX A (CONT'D)

APPENDIX B

REFERENCES - MILITARY PUBLICATIONS

The following publications are applicable to operators, organizational, direct support and general support maintenance of Test Set, Integrated Circuit Card AN/USM-371.

DA PAM 310-4	Index of Technical Publications, Technical Manuals, Technical Bulletins, Supply Manuals (Type 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
DA PAM 310-7	US Army Index of Modification Work Orders.
CTA 50-970	Expendable Items: (Except Medical, Class V, Repair Parts ant Heraldic Items).
SB 708-42	Federal Supply Code for Manufacturers United States and Canada Code to Name (Cataloging Handbook H4-2).
TB 11-6600-252-10-1	Supplementary Operating Instructions, Test Sets, Integrated Circuit Card Tester AN/USM-371 ant AN/USM-37LA, Volume I (Test Programs for AUTODIN Printed Circuit Carla No. A52602 Through A65089).
TB 11-6600-252-10-2	Supplementary Operating Instructions, Test Sets, Integrated Circuit Card Tester AN/USM-371 and AN/USM-371A, Volume II (Test Programs for AUTODIN Printed Circuit Cards No. A65093 Through A65441).
TB 11-6600-252-10-3	Supplementary Operating Instructions, Test Sets, Integrated Circuit Card Tester AN/USM-371 and ANlUSM-371A, Volume III (Test Programs for AUTODIN Printed Circuit Cards No. SM-E-546367 Through SM-E-546584).
TB 11-6600-252-10-4	Supplementary Operating Instructions, Test Sets, Integrated Circuit Card Tester AN/USM-371 and AN/USM-371A, Volume IV (Test Programs for AUTODIN Printed Circuit Cards No. SM-E-546587 Through SM-E-546840).
TB 11-660-252-10-5	Supplementary Operating Instructions, Test Sets, Integrated Circuit Card Tester AN/USM-371 and AN/USM-371A, Volume V (Test Programs for AUTODIN Printed Circuit Cards No. 1115301 Through 56736G1).

TB 11-6600-252-10-6	Supplementary Operating Instructions, Test Sets, Integrated Circuit Cart Tester AN/USM-371 and AN/USM-37LA, Volume V1 (Printed Circuit Card Test Programs for Teletypewriter Control Unit C-7050/G (Cards PL-1139/G Through PL-1158/G) and Modem, Low Speed Wire Line MD-674/G (Cards A-1 Through A-20, AX, and A33A2)).
TB 11-6600-252-10-7	Supplementary Operating Instructions, Test Sets, Integrated Circuit Card Tester AN/USM-371 and AN/USM-371A, Volume VII (Printed Circuit Card Test Programs for Synchronizer, Electrical SN-394(V)/G (Cards A-1 Through A-6) and for Routing Set, Teletypewriter AN/FGC-73(V) (Cards 200000G1 Through 200160G1)).
TB 43-0118	Field Instructions for: Painting and Preserving Electronics Command Equipment.
TM 11-6625-654-14	Operator's, Organizational, Direct Support, and General Support Maintenance Manual (Including Repair Parts and Special Tools Lists) for Multimeter AN/USM-223.
TM 11-6625-2577-24P	Organizational, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), Test Sets, Integrated Circuit Card AN/USM-371 and AN/USH-371A.
TM 11-6625-2594-14	Operator's, Organizational, Direct Support, and General Support Maintenance Manual for Test Set, Integrated Circuit Card AN/USM-371A (Dynatronics Model ICT-103).
TM 11-6625-2658-14	Operator's, Organizational, Direct Support, and General Support Maintenance Manual for Oscilloscope AN/USM-281C.
TM 38-750	The Army Maintenance Management Systems (TAMMS).
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

APPENDIX C

MAINTENANCE ALLOCATION

Section I. INTRODUCTION

C-1. General

This appendix provides a summary of the maintenance operations for Test Set Integrated Circuit Card AN/USM-371. It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning main" tenance operational.

C-2. Maintenance Function

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable element of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly) end item, or system.

j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable

equipment to a like new condition in accordance with original manufacturing standards. Rebuild is degree of material maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

C-3. Column Entries

a. Column 1, Group Number. Column 1 fiats group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column 2, Component/Assembly. Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. Column 8, Maintenance Functions. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4, Maintenance Category. Column 4 specifies, by the listing of a "work time" figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 8. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate "work time" figures will be shown for each category. The number of task-hours specified by the "work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chum Subcolumns of column 4 are as follows:

C- Operator/Crew
O- Organizational
F- Direct Support
H- General Support
D- Depot

e. Column 5, Tools and Equipment. Column 6 specifies by code, those common tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetical code which leads to the remark in section IV, Remarks, which is pertinent to the item opposite the particular code.

C 4. Tool and Test Equipment Requirements (Sec III)

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lisp the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (6-digit) in parentheses.

C-5. Remarks (Sec IV)

a. Reference Code. This code refers to the appropriate item in section II, column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in section II

SECTION II MAINTENANCE ALLOCATION CHART FOR TEST SET, INTEGRATED CIRCUIT CARD, AN/USM-371

(1) Group Number	(2) Component/ Assembly	(3) Maintenance Function	(4) Maintenance Level C	O	F	H	D	(5) Tools and Equipment	(6) Remarks
00	TEST SET, INTEGRATED CIRCUIT CARD AN/USM-371	INSPECT		0.5					A
	TEST			1.0				1	B
	TEST					2.0		1, 3-6, 11-12	
	SERVICE			1.0				2	
	ADJUST					1.5		1, 2	
	REPAIR			1.0				1	C
	REPAIR					2.5		1-12	
	OVERHAUL						8.0	1-12	
01	CARD TESTER ASSEMBLY, CHASSIS A1								D
0101	CIRCUIT CARD ASSEMBLY, A1A1	REPLACE				0.5		2	
		REPAIR				1.0		1-5, 11, 12	
0102	CIRCUIT CARD ASSEMBLY A1A2								E
0103	CIRCUIT CARD ASSEMBLY A1A3								E
0104	CIRCUIT CARD ASSEMBLY A1A8								E
0105	CIRCUIT CARD ASSEMBLY A1A9								E
0106	CIRCUIT CARD ASSEMBLY, A1A4, A1A5								E
0107	CIRCUIT CARD ASSEMBLY, A1A7								E
0108	CIRCUIT CARD ASSEMBLE, A1A6								E
0109	CONNECTOR PLATE ASSEMBLY, A1A11								D
0110	PANEL ASSEMBLY, FRONT, A1A12								D
011001	READER, PUNCHED CARD, A1A12A2	REPAIR				2.0		1, 2, 7-10	
	SERVICE					0.3		2	
	ADJUST					1.0		1, 2	
01100101	READER, PUNCHED CARD, A1A12A2A1								D
0111	POWER SUPPLY ASSEMBLY, A1PS1	REPAIR				2.0		1, 2, 6	
	ADJUST					0.5		1, 6	
011101	CIRCUIT CARD ASSEMBLY, A1PS1A1								E

SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS FOR TEST SET, INTEGRATED CIRCUIT CARD AN/USM-371

Tool or Test Equipment Ref Code	Maintenance Category	Nomenclature	National/Stock National/NATO Stock Number	Tool Number
1	O, H, D	MULTIMETER, AN/USM-223	6625-00-999-7465	
2	O, H, D	TOOL KIT, ELECTRONIC EQUIPMENT TK-100/G	5180-00-605-0079	
3	H, D	OSCILLOSCOPE, AN/USM-281C	6625-00-106-9622	
4	H, D	CART, OSCILLOSCOPE WITH CABINET (TEKTRONIX LAB CART MODEL NO. 3)		
5	H, D	PROBE, TIP, COIL SPRING (TEKTRONIX INC. NO. 206-0061-00)- 2 EACH	6625-00-054-0231	
6	H, D	VOLTMETER, DIGITAL (HEWLETT-PACKARD MULTIMETER NO. 34702A and DISPLAY NO. 34750A060)	6625-00-032-5862	
7	H, D	WRAPPING TOOL, WIRE (GARDNER-DENVER NO. 14R2-F)	5130-00-919-3486	
8	H, D	BIT, WIRE WRAP (GARDNER-DENVER NO. 502128)	5130-00-091-0766	
9	H, D	SLEEVE, ELECTRICAL (GARDNER-DENVER NO. 502129)	5970-00-179-8062	
10	H, D	TOOL, HAND WIRE UNWRAPPING (GARDNER-DENVER NO. 500130	5120-00-104-9022	
11	H, D	EXTENDER BOARD, DYNATRONICS NO. 08-900700		
12	H, D	TEST SET, AN/USM-371	6625-00-431-8440	

SECTION IV. REMARKS

Reference Code	Remarks
A	External.
B	Organizational test is limited to equipment operation.
C	Organizational repair is limited to replacement of A1A12 jack tips, indicator lights and lamps, and A1PS1 fuses.
D	Components with no maintenance functions are repaired under the next higher assembly/end item.
E	Maintenance Function, Maintenance Category, and Tools and Equipment are the same as that for the group 0101.

By Order of the of the Army:

E. C. MEYER
General, United States Army
Chief of Staff

Official:

J. C. PENNINGTON
Major General, United States Army
The Adjutant General

☆U.S. GOVERNMENT PRINTING OFFICE: 1984-484-1/20107

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The Metric System and Equivalents

Linear Measure

1 centimeter = 10 millimeters = .39 inch
1 decimeter = 10 centimeters = 3.94 inches
1 meter = 10 decimeters = 39.37 inches
1 dekameter = 10 meters = 32.8 feet
1 hectometer = 10 dekameters = 328.08 feet
1 kilometer = 10 hectometers = 3,280.8 feet

Weights

1 centigram = 10 milligrams = .15 grain
1 decigram = 10 centigrams = 1.54 grains
1 gram = 10 decigram = .035 ounce
1 decagram = 10 grams = .35 ounce
1 hectogram = 10 decagrams = 3.52 ounces
1 kilogram = 10 hectograms = 2.2 pounds
1 quintal = 100 kilograms = 220.46 pounds
1 metric ton = 10 quintals = 1.1 short tons

Liquid Measure

1 centiliter = 10 milliters = .34 fl. ounce
1 deciliter = 10 centiliters = 3.38 fl. ounces
1 liter = 10 deciliters = 33.81 fl. ounces
1 dekaliter = 10 liters = 2.64 gallons
1 hectoliter = 10 dekaliters = 26.42 gallons
1 kiloliter = 10 hectoliters = 264.18 gallons

Square Measure

1 sq. centimeter = 100 sq. millimeters = .155 sq. inch
1 sq. decimeter = 100 sq. centimeters = 15.5 sq. inches
1 sq. meter (centare) = 100 sq. decimeters = 10.76 sq. feet
1 sq. dekameter (are) = 100 sq. meters = 1,076.4 sq. feet
1 sq. hectometer (hectare) = 100 sq. dekameters = 2.47 acres
1 sq. kilometer = 100 sq. hectometers = .386 sq. mile

Cubic Measure

1 cu. centimeter = 1000 cu. millimeters = .06 cu. inch
1 cu. decimeter = 1000 cu. centimeters = 61.02 cu. inches
1 cu. meter = 1000 cu. decimeters = 35.31 cu. feet

Approximate Conversion Factors

To change	*To*	*Multiply by*	*To change*	*To*	*Multiply by*
inches	centimeters	2.540	ounce-inches	Newton-meters	.007062
feet	meters	.305	centimeters	inches	.394
yards	meters	.914	meters	feet	3.280
miles	kilometers	1.609	meters	yards	1.094
square inches	square centimeters	6.451	kilometers	miles	.621
square feet	square meters	.093	square centimeters	square inches	.155
square yards	square meters	.836	square meters	square feet	10.764
square miles	square kilometers	2.590	square meters	square yards	1.196
acres	square hectometers	.405	square kilometers	square miles	.386
cubic feet	cubic meters	.028	square hectometers	acres	2.471
cubic yards	cubic meters	.765	cubic meters	cubic feet	35.315
fluid ounces	milliliters	29,573	cubic meters	cubic yards	1.308
pints	liters	.473	milliliters	fluid ounces	.034
quarts	liters	.946	liters	pints	2.113
gallons	liters	3.785	liters	quarts	1.057
ounces	grams	28.349	liters	gallons	.264
pounds	kilograms	.454	grams	ounces	.035
short tons	metric tons	.907	kilograms	pounds	2.205
pound-feet	Newton-meters	1.356	metric tons	short tons	1.102
pound-inches	Newton-meters	.11296			

Temperature (Exact)

°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

PIN: 046276-000